IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

POWER INTEGRATIONS, INC., Plaintiff, v. FAIRCHILD SEMICONDUCTOR INTERNATIONAL, INC., and FAIRCHILD SEMICONDUCTOR CORPORATION, Defendants.	)	**REDACTED PUBLIC VERSION** C.A. No. 04-1371-JJF

COMBINED APPENDIX TO DEFENDANTS': (i) OPENING POST-TRIAL BRIEF IN SUPPORT OF THEIR ASSERTION THAT THE PATENTS-IN-SUIT ARE UNENFORCEABLE DUE TO INEQUITABLE CONDUCT; AND (ii) PROPOSED FINDINGS OF FACT AND CONCLUSIONS OF LAW REGARDING THE UNENFORCEABILITY OF THE PATENTS-IN-SUIT DUE TO INEQUITABLE CONDUCT

(VOLUME III of V)

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Dated: November 5, 2007

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DX 1001, PWR-SMP211, PWM Power Supply IC, 85-265 VAC Input, Isolated, Regulated DC Output

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DX 1003, Power Integrations' Responses and Objections to Defendants' Third Set of Requests for Admission (Nos. 44-50)

DX 1004, Form 10-Q, Filed 11/7/05 for Period Ending 9/30/05

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VOLUME V

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DX 110

REDACTED

DX 113

INVENTION DISCLOSURE FORM
POWER INTEGRATIONS-COMPANY PRIVATE

INVENTOR (S):

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Citizenship USA Social Security #

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Phone: Work: (408) 523-9223 Home: REDACTED
Citizenship Sweden Social Security #

NAME OF THE INVENTION: Fully Integrated softstart & frequency jitter for offline PWM Switch
DATE OF THE INVENTION: 8-26-97
DATE OF DISCLOSURE TO OTHERS IN THE COMPANY: 9-2-97
LIST OF THEIR NAMES: David Kung
Erdem Bircan
Derek Kroes

DOES A PRACTICAL IMPLEMENTATION OF THE INVENTION EXIST? Yes

Case No. 04-1371-JJF
DEFT Exhibit No. DX 113
Date Entered
Signature

1

PIF 63314
HIGHLY CONFIDENTIAL - OUTSIDE COUNSEL ONLY

IF SO IN WHAT FORM? simulations

NAME OF THE PRODUCT (S) USING THIS INVENTION: TOPSwitch III

EXPECTED DATE OF FIRST SAMPLING: Q3, 1998

EXPECTED DATE OF FIRST SALE: Q4, 1998

EXPECTED DATE OF FIRST PUBLIC DISCLOSURE (EX. ARTICLE, PRESENTATION AT CUSTOMER ETC.): March 1998

WHAT PROBLEM DOES THIS INVENTION SOLVE: Provides a completely integrated softstart and frequency jitter functions for off-line PWM Switch. These functions in general require large time constants and therefore are not easily integrated in an IC. By using the same timing element circuit for both functions, and using very low current sources, the silicon area is kept to absolute minimum. The frequency jitter reduces the Electromagnetic Interference (EMI) thereby enabling smaller filter to suppress EMI emissions. Softstart reduces instantaneous stress on many components during power-up, thereby reducing the cost of these components.

DESCRIPTION OF THE PRIOR ART IF ANY (USE ADDITIONAL PAGES IF NEEDED):

Frequency jitter is not commonly used in power supplies. In some cases a resistor is used from the storage capacitor to the frequency setting resistor to modulate the oscillator current with line voltage ripple. This approach is not accurate

since the ripple varies a lot with line and load variations. Also, its modulating frequency is 60Hz, which may not be the optimum modulating jitter frequency. 120Hz

Softstart is implemented using external capacitor.

DESCRIPTION OF THE INVENTION (USE ADDITIONAL PAGES IF NEEDED):

This invention uses a monolithic low frequency oscillator. This is accomplished by utilizing a very low current source to charge and discharge an on-chip capacitor.

During power-up the oscillator is held low. As soon as the chip is ready to switch, the oscillator is released to oscillate. The first rising edge of the oscillator is used to slowly increase the maximum duty cycle.

The low frequency oscillator's sawtooth output is also used to generate a current source proportional to its output voltage. This current source is added to the main current source of the PWM oscillator to modulate its frequency. (see diagrams)

SIGNATURE OF THE INVENTOR (S):

1. Balu Balakrishnan Date: 3-26-98

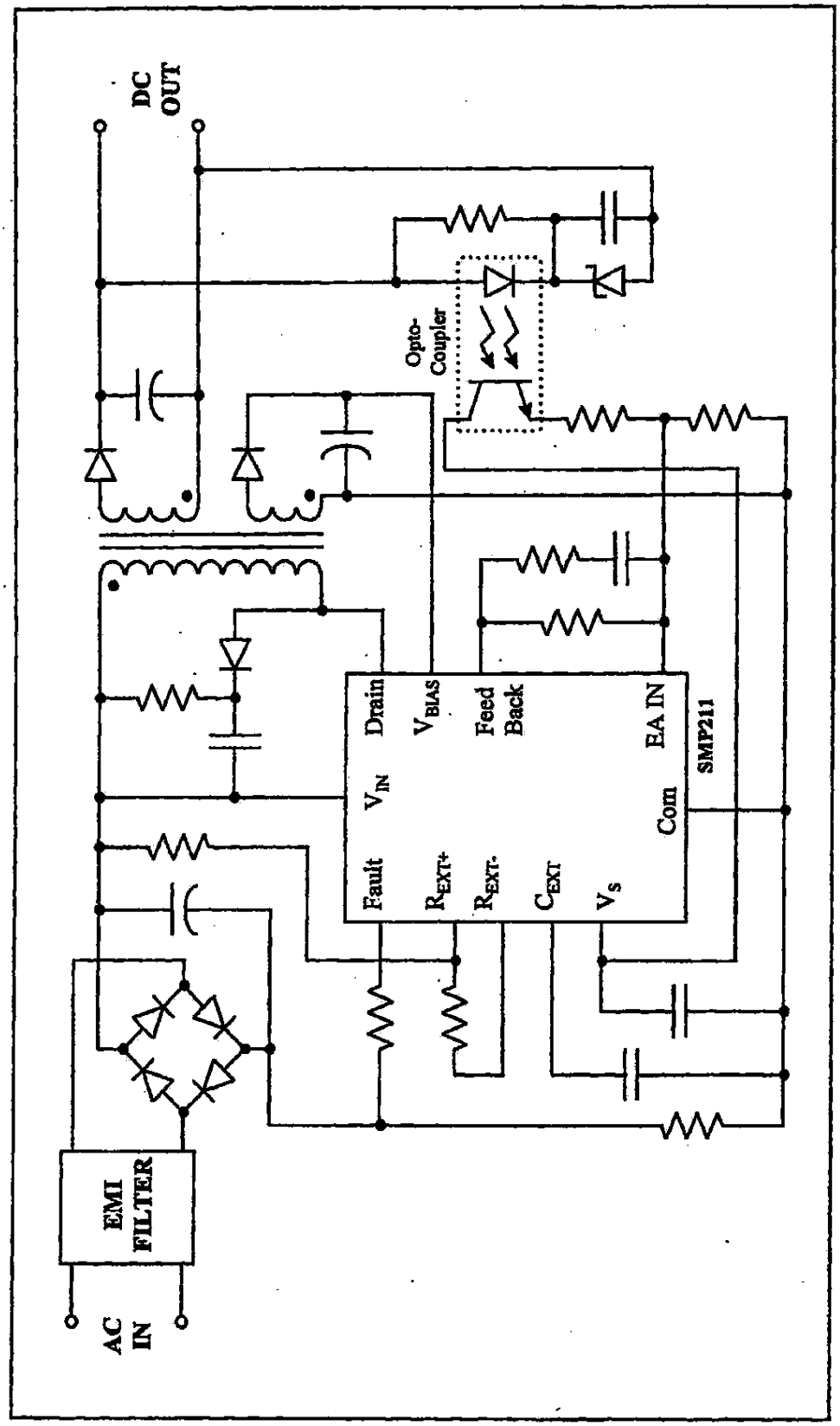
2. Alex Djenguerian Date: 3-25-98

3. Leif Lund Date: 04-02-98

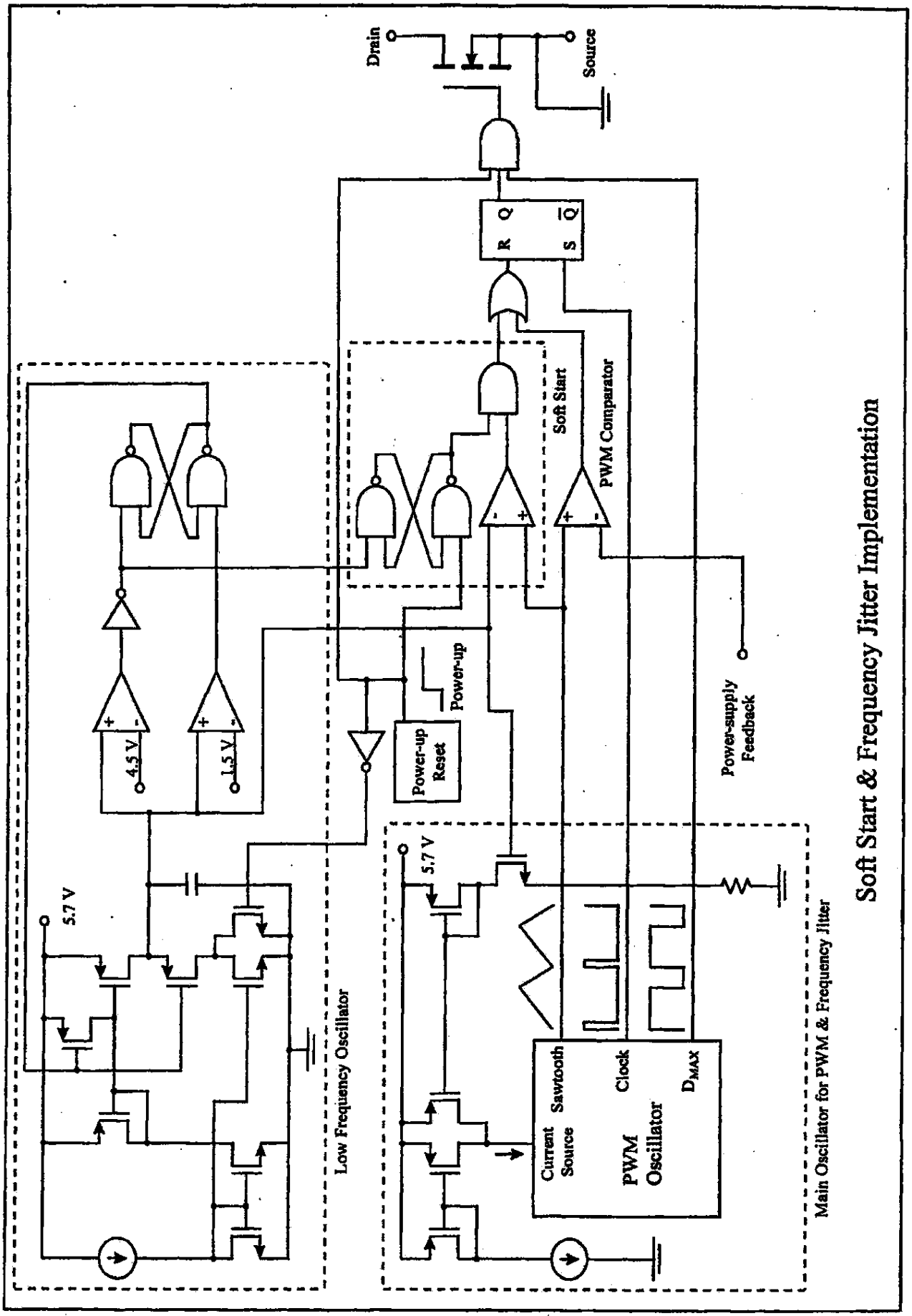
UNDERSTOOD AND WITNESSED BY;

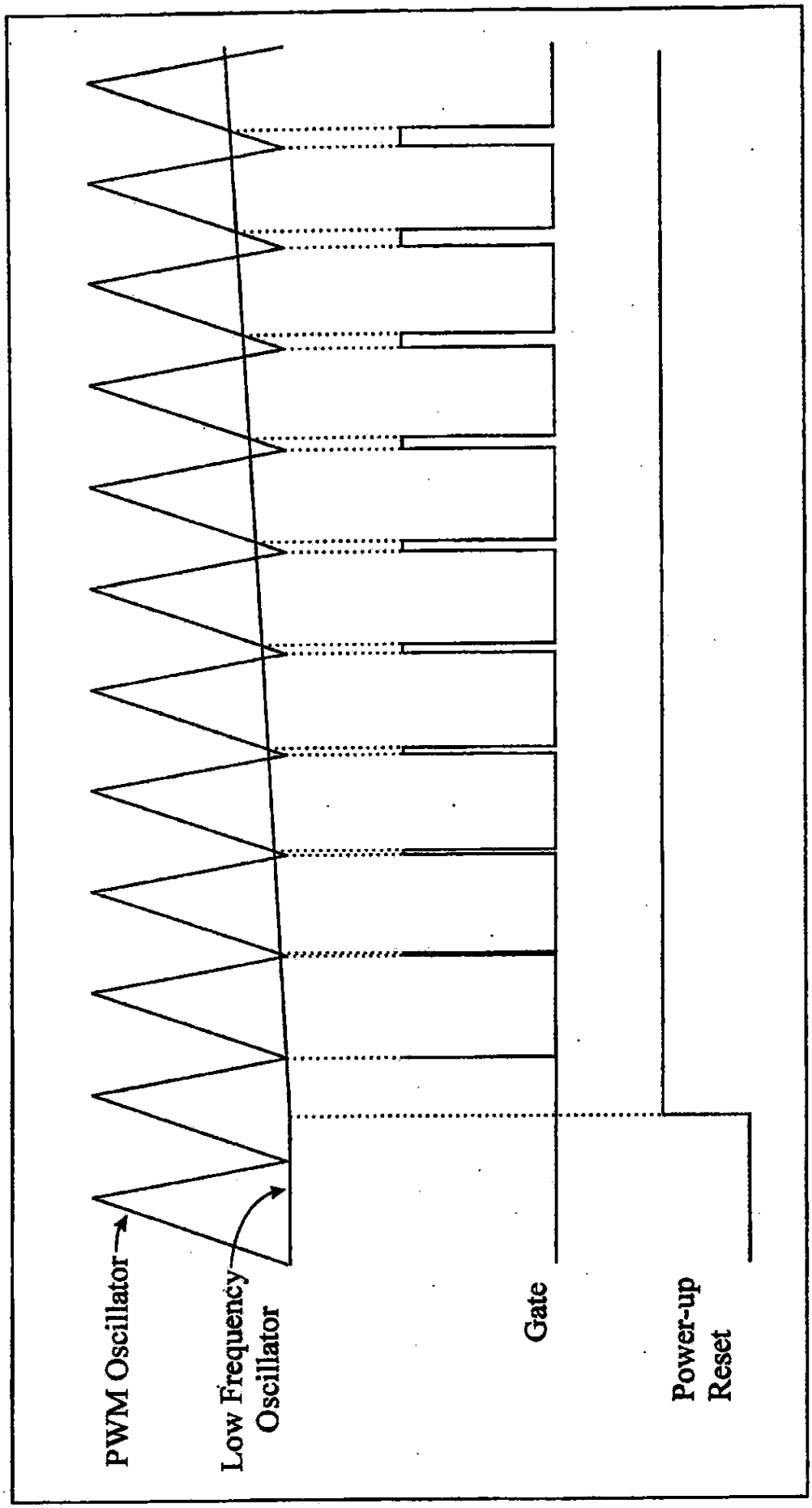
NAME Erdem Bircan Signature /s/ Bircan Date 3/26/98

NAME DAVID KUNG Signature David Kung Date 3-24-98

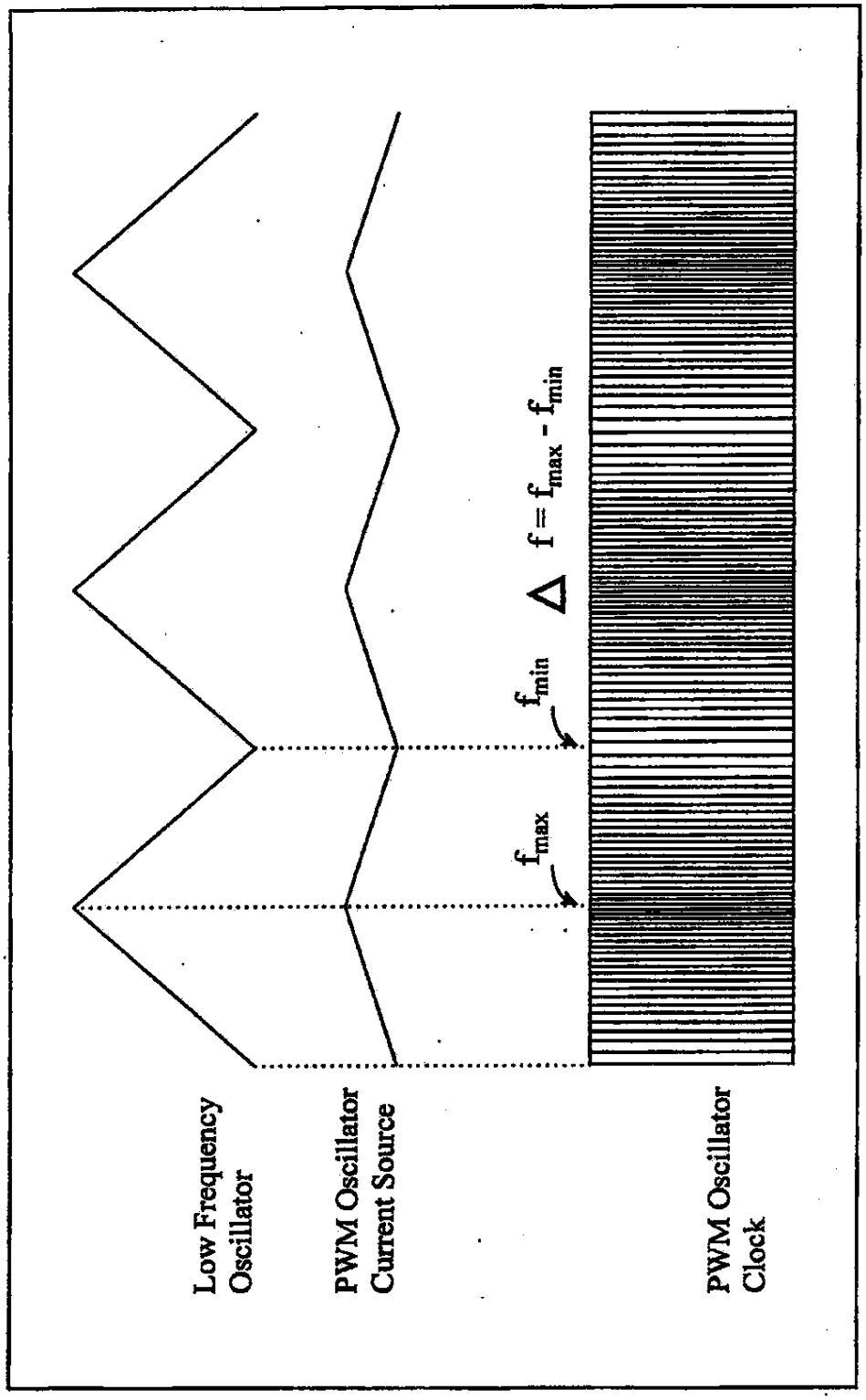


Previous Application of Soft Start & Frequency Jitter

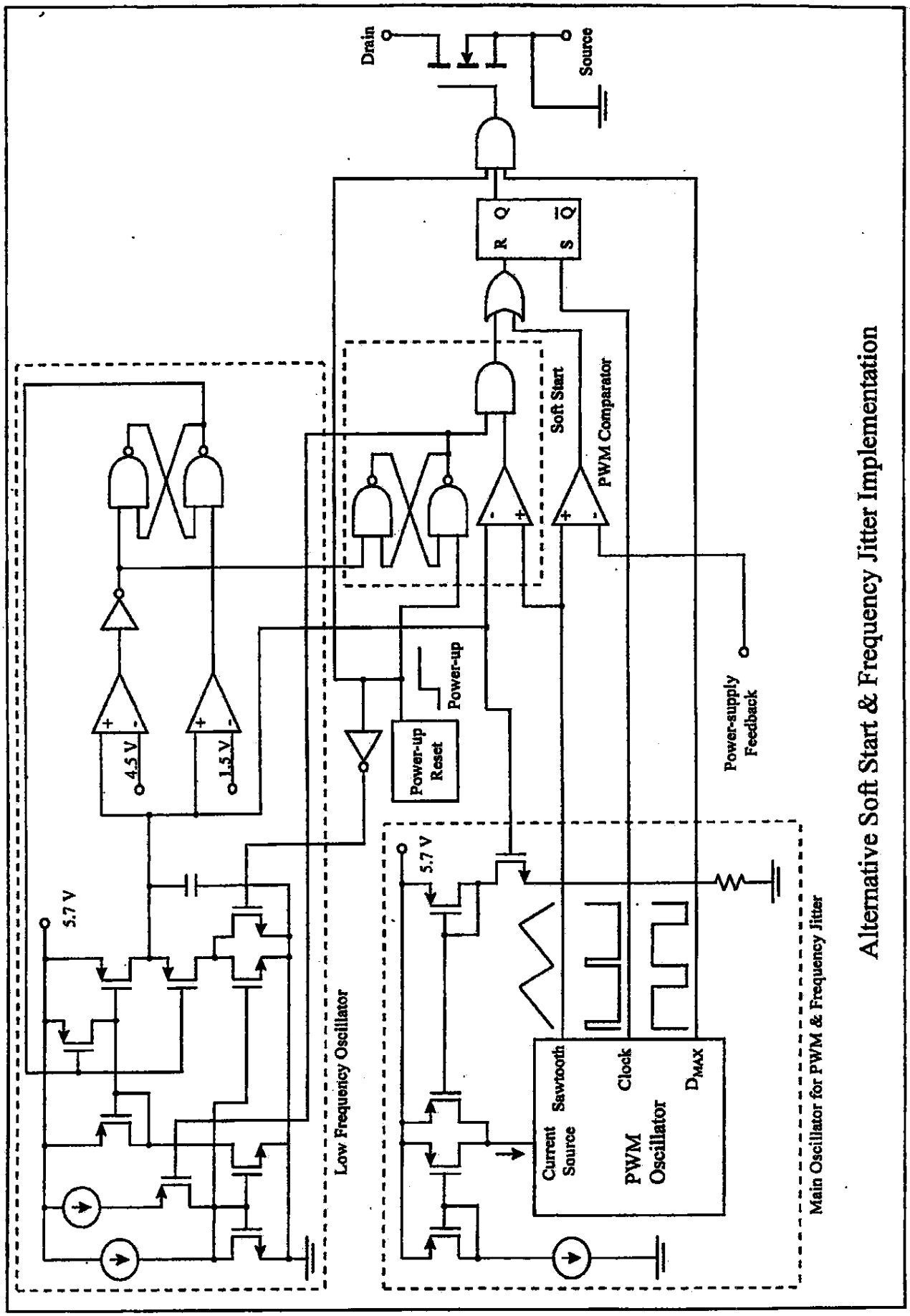

Drain
Source
R
S
Q
$\overline{Q}$
Soft Start
PWM Comparator
Power-up
Power-up Reset
Power-supply Feedback
4.5 V
1.5 V
5.7 V
5.7 V
Low Frequency Oscillator
Main Oscillator for PWM & Frequency Jitter
Current Source
Sawtooth
Clock
D_{MAX}
PWM Oscillator
Soft Start & Frequency Jitter Implementation

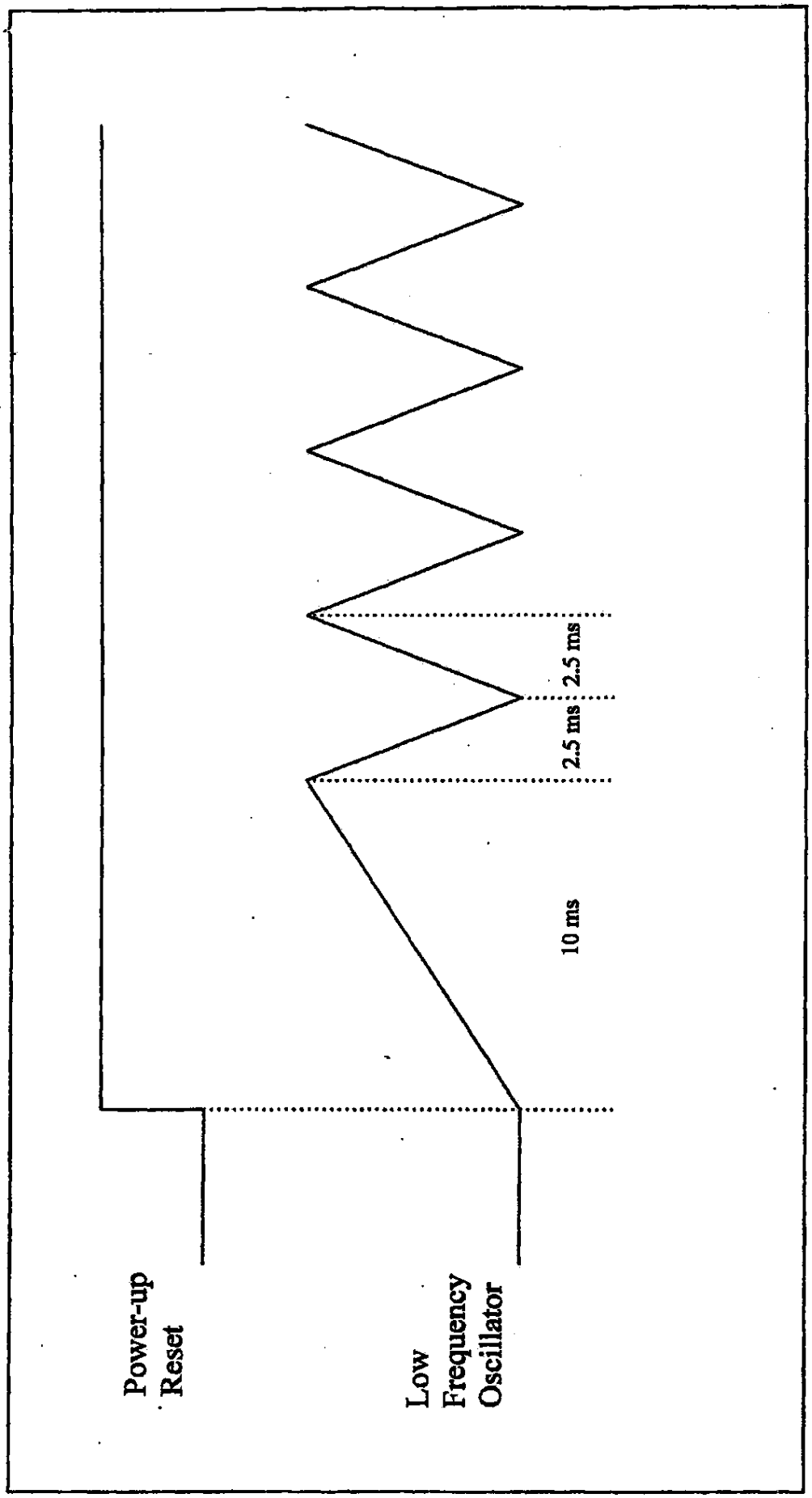


Soft Start Timing

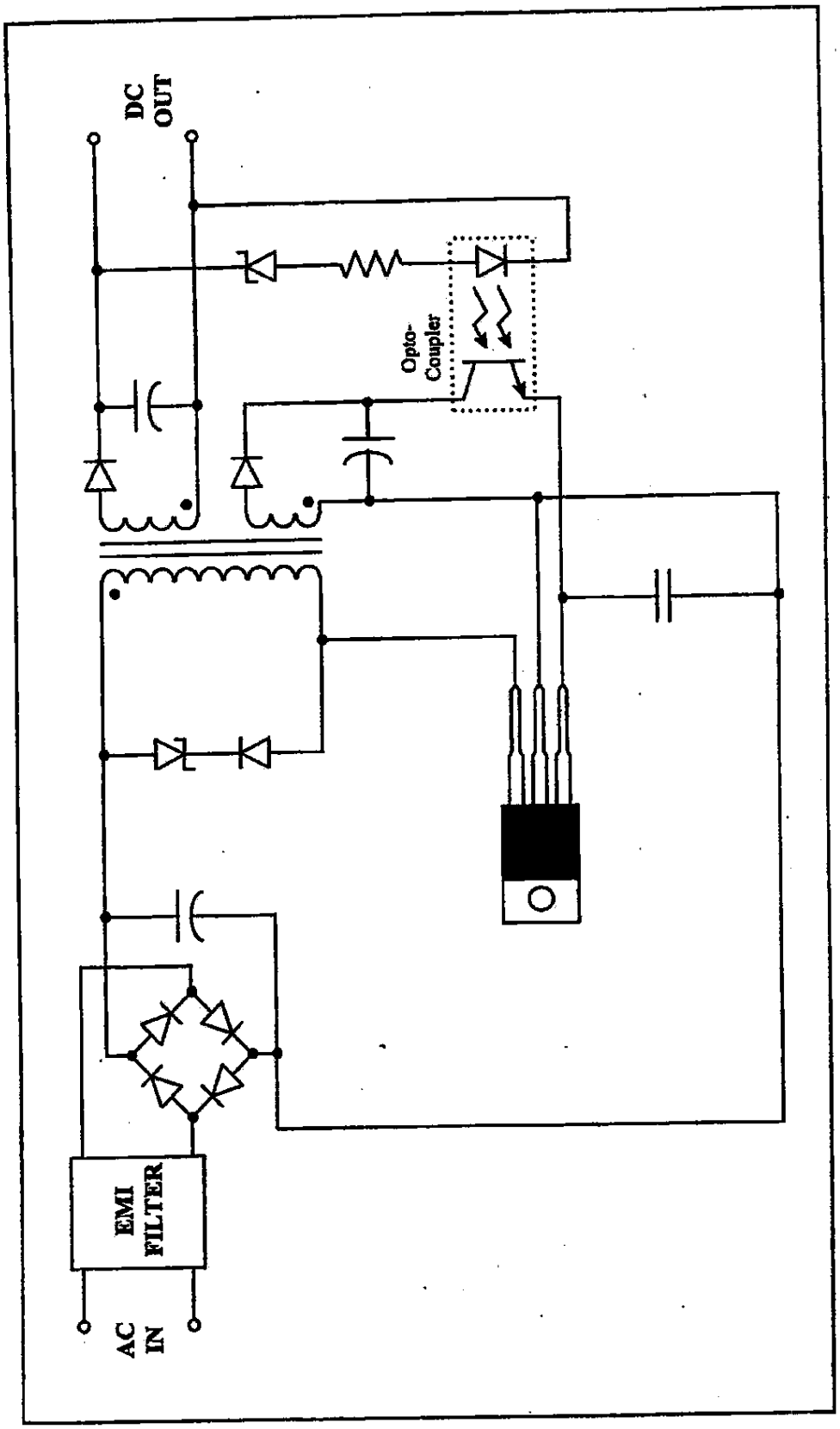


Frequency Jitter Timing


Drain
Source
Q
R
S
Soft Start
PWM Comparator
Power-up
Power-up Reset
Power-supply Feedback
4.5 V
1.5 V
5.7 V
Low Frequency Oscillator
Main Oscillator for PWM & Frequency Jitter
Current Source
Sawtooth
Clock
D_{MAX}
PWM Oscillator
Alternative Soft Start & Frequency Jitter Implementation



Low Frequency Oscillator Timing with Alternative Approach



Power Supply with Integrated Soft Start & Frequency Jitter

DX 114

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DX 115

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DX 116

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DX 118

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DX 119

REDACTED

DX 120

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DX 121

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DX 122

PWR-SMP260

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 60 W from rectified 220/240 VAC input, 30 W from universal (85 to 265 VAC) input
- Feedforward control for constant-power battery charging
- External transformer provides isolation and selectable output voltages

High-speed Current-mode PWM Controller
- Leading edge current blanking
- Selectable maximum duty cycle - 50% or 90%
- Internal pre-regulator self-powers the IC on start-up
- Wide bias voltage range - 10-30 V
- Direct connection to optocoupler feedback
- Programmable slope compensation
- Low-current standby mode

Built-In Self-protection Circuits
- Full cycle soft-start - Linear ramp up of switching current
- Shutdown on fault with automatic restart
- Adjustable current limit
- Regulates from zero load to full load
- Undervoltage lockout
- Thermal shutdown

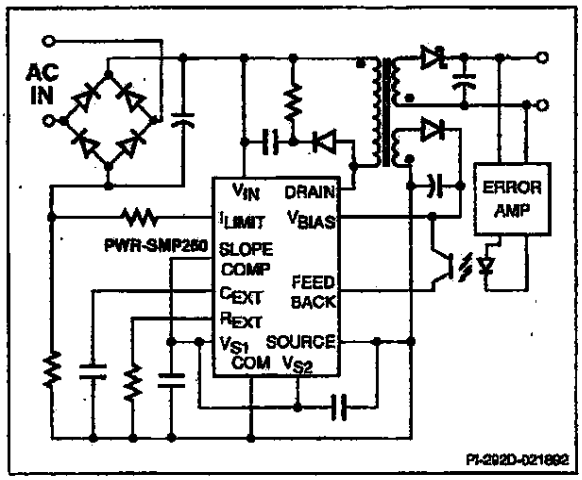


Figure 1. Typical Application

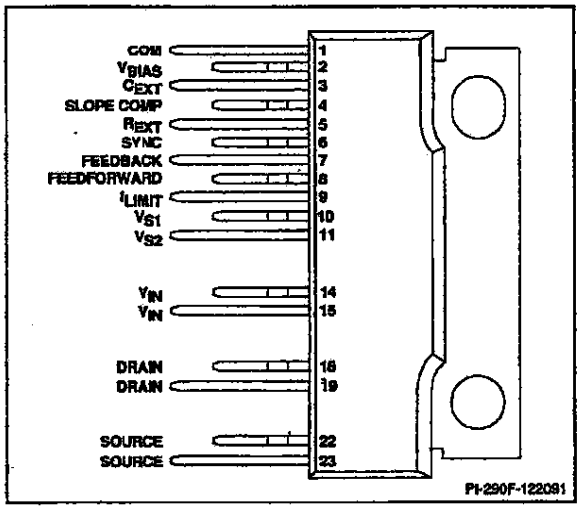


Figure 2. Pin Configuration

Description

The PWR-SMP260, intended for 220/240 VAC or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The current-mode PWM controller section of the PWR-SMP260 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, summing junction, PWM comparator, gate driver, soft-start, and circuit protection. The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage.

The PWR-SMP260 is available in a plastic power SIP package. A surface mount power package version will be available in the second half of 1992.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP260WTC	23-pin PWR SIP	0 to 70°C

411 Clyde Avenue
Mountain View, California, 94043
Phone: (415) 960-3572
Applications Hotline: (800) 552-3155
FAX: (800) 468-0809 In CA: (415) 940-1541

PRELIMINARY

February 1992

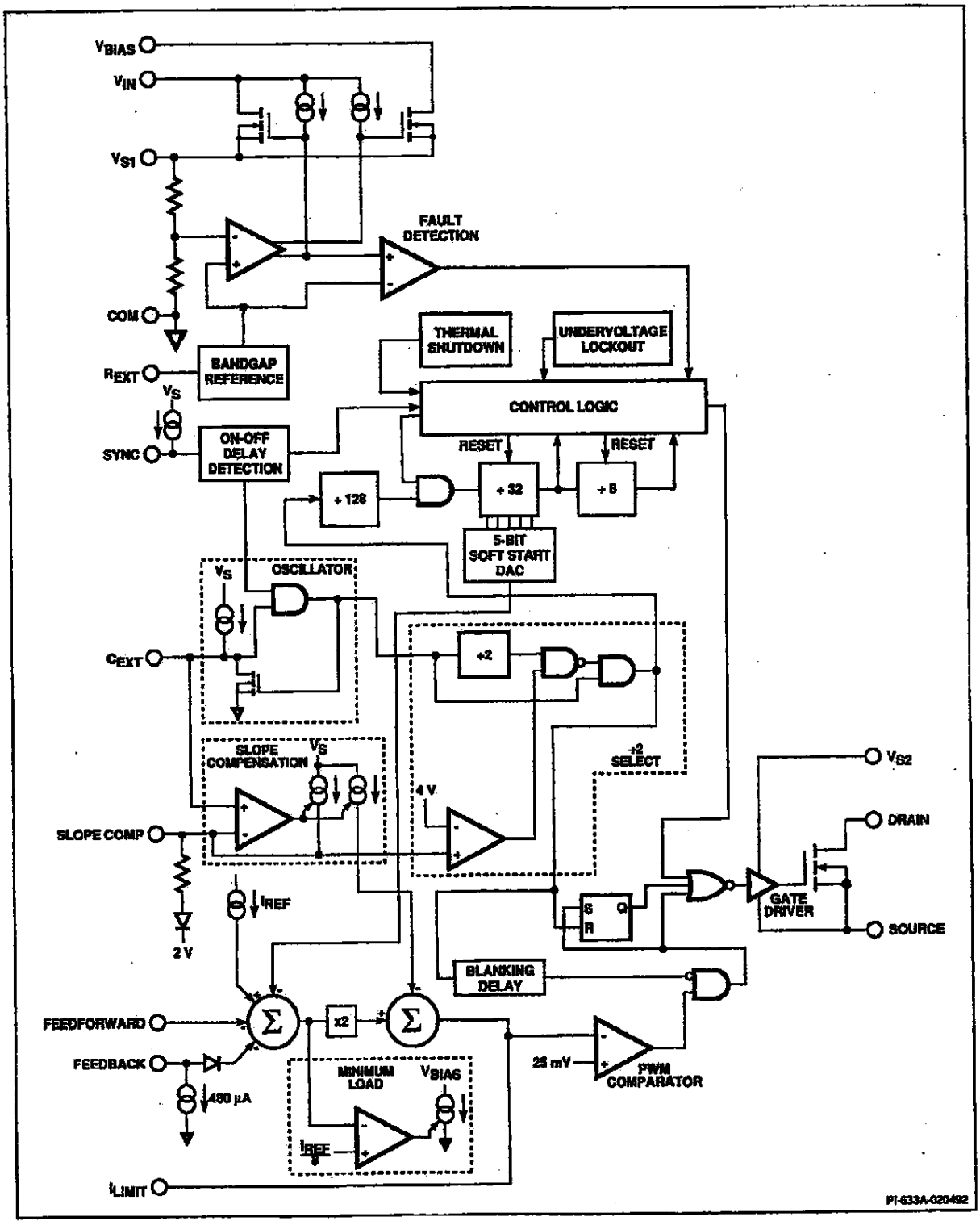


Figure 3. Functional Block Diagram of the PWR-SMP260.

Pin Functional Description

Pin 1:
COM is common reference point for all low-power and reference circuitry.

Pin 2:
V_{BIAS} is the bootstrap supply voltage proportional to the output voltage used to self-power the device once the supply is operating.

Pin 3:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance between C_{EXT} and COM linearly decreases the PWM frequency.

Pin 4:
SLOPE COMP is used to select the amount of slope compensation to be injected into the summing junction in the maximum duty cycle mode. Connecting the pin to V_S selects 50% mode, and connction through a resistor to COM selects the 95% mode.

Pin 5:
A resistor placed between R_{EXT} and ANALOG COM sets the internal bias currents.

Pin 6:
SYNC is an active-low input with an internal pull-up used for synchronizing the oscillator. A continuous low level turns off the power supply output.

Pin 7:
FEEDBACK accepts current from an opto-coupler connected directly from V_{BIAS} which is controlled by an output-referenced error amplifier.

Pin 8:
FEEDFORWARD accepts current from an input voltage compensation resistor to automatically adjust the duty cycle for changes in input voltage.

Pin 9:
I_{LIMIT} is the output of the summing junction. Current flowing from this pin through a resistor will set the current comparator threshold.

Pin 10:
V_{S1} is the output of the internal V_{IN} and V_{BIAS} regulators. Connection to V_{S2} and an external bypass capacitor to COM is required for proper operation.

Pin 11:
The output gate drive circuit receives power via V_{S2}. Connection to V_{S1} and an external bypass capacitor to SOURCE is required for proper operation.

Pin 14, 15:
V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 18, 19:
Open **DRAIN** of the output MOSFET.

Pin 22, 23:
The **SOURCE** is the high-current return for the output MOSFET.

PWR-SMP260 Functional Description

Off-line Linear and Bias Regulators
The off-line linear regulator powers the control circuits when the boot-strap bias voltage cannot. The off-line and bias linear regulator contains two high voltage MOSFETs, a gate bias current source, and an error amplifier. The error amplifier regulates V_S from either the off-line rectified voltage or the bias supply voltage, the bias supply voltage has preference to minimize power consumption.

The off-line linear regulator MOSFET dissipates significant amounts of power when supplying the bias current. When the V_{BIAS} voltage is greater than the V_{BIAS} threshold voltage the off-line linear regulator is cut off and internal bias current is supplied by the V_{BIAS} supply, decreasing the dissipation in the off-line regulator

V_{S1} is the output of the bias regulator and supplies power to all internal analog circuits. An external bypass capacitor connected between V_{S1} and SOURCE is required for filtering and noise reduction. V_{S2} is the power supply connection for the gate drive circuitry, and must be connected externally to V_{S1}. V_{S1} and V_{S2} are not internally connected.

Bandgap Reference
The reference voltage is generated by the temperature compensated bandgap reference and buffer. The voltage is used for setting thresholds for the current-mode regulator, soft-start, and over-temperature circuits. R_{EXT} is used by this circuit to provide precision current sources from the reference voltages.

PWR-SMP260 Functional Description (cont.)

Oscillator
The oscillator frequency is determined by the value of the external timing capacitor (C_{EXT}). An internal current source slowly charges C_{EXT} to a maximum. C_{EXT} is then rapidly discharged to its initial value.

When the oscillator frequency is being selected care should be taken to determine the selected maximum duty cycle. If the 50% maximum duty cycle option is selected the oscillator will need to operate at twice the output frequency. The slope compensation pin is used to select available maximum duty cycle.

The oscillator frequency can be synchronized to an external signal by applying a short synchronizing pulse to the SYNC pin. The free-running frequency of the oscillator must be set lower than the minimum synchronizing frequency.

The power supply can be turned off by holding the SYNC pin continuously low. When turned off, the power consumption of the control circuit is reduced to minimize standby power dissipation.

Pulse Width Modulator
The pulse width modulator combines the current sensing comparator, latch, and current summing junction functions.

The summing junction combines currents from the soft-start digital to analog converter current source, the slope compensation circuit, the feedback input and the feedforward input. The output of the summing junction is a current source. Current flowing from this pin through a resistor will set the current mode comparator threshold.

The current mode comparator sets the R-S flip-flop and turns off the output transistor when the voltage on the input to the current mode comparator falls to 25 mV. The current mode comparator input will be at 25 mV when the primary current reaches the desired peak value. The R-S flip-flop holds the output transistor off until the next cycle is ready to begin.

The feedback signal is diode coupled into the summing junction and a bias current source is provided so that an optical coupler can be DC biased without the addition of any external components. The feedback, feedforward, soft-start digital to analog converter and slope compensation current signals all reduce the current flowing from the output of the summing junction. The pulse width modulator adjusts the duty cycle to match the peak switch current with the scaled I_{LIMIT} current, as shown in Figure 4(a). The slope compensation current signal linearly reduces the instantaneous current flowing from the output of the summing junction over the cycle.

Slope compensation should be used when the maximum duty cycle exceeds 50%. The amount of slope compensation required is inversely related to the magnetizing current flowing in the output transistor. Figure 4(b) gives the relationships between the feedback current and the I_{LIMIT} current with an external slope compensation resistor. Refer to AN-11 for more detailed information on selecting slope compensation components.

Leading edge blanking of the current-mode comparator is provided by inhibiting the output of the comparator for a short time after the output transistor is turned on. The leading edge blanking time has been set so that ultra fast recovery rectifiers operating at their specified recovery times will not cause premature termination of the switching pulse.

The active minimum load circuit senses when the sum junction current is less than 12% of maximum sum junction current and increases the power consumption of the control circuit to maintain this minimum load power level. This will prevent the programmed current from falling to such a low level that the required pulse width would approach the blanking time.

Full Function Soft-Start
The soft-start circuit controls the pulse width modulator when the power supply is in a fault condition as demonstrated in Figure 5. During the time that the fault condition exists, the power supply will be enabled one eighth of the time. When the power supply is enabled, the I_{LIMIT} current ramps up from zero to the maximum value over 4096 cycles of the power supply. A 5-bit digital to analog converter current source controls the value of the Ilimit current and the output switch current. The controlled ramp up of the switch current limits the power stresses on the output diode rectifier and prevents the transformer from being driven into saturation.

The soft-start determines an output fault has occurred if the V_{BIAS} voltage is less than the V_{BIAS} threshold voltage after the soft-start ramp up time. During a fault condition, the output transistor is turned off for a period of 28,672 cycles of the power supply, after which the fault condition is tested by ramping up the switch current to full scale. If V_{BIAS} is not above the V_{BIAS} threshold voltage by the time full current is reached the fault condition is again detected and the switch is turned off.

Undervoltage Protection Circuit
The undervoltage protection circuit insures that the output transistor is off until the V_{SI} voltage is regulated.

Overtemperature Protection Circuit
The overtemperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 140°C). The device will turn back on again when the junction has cooled past the hysteresis temperature level.

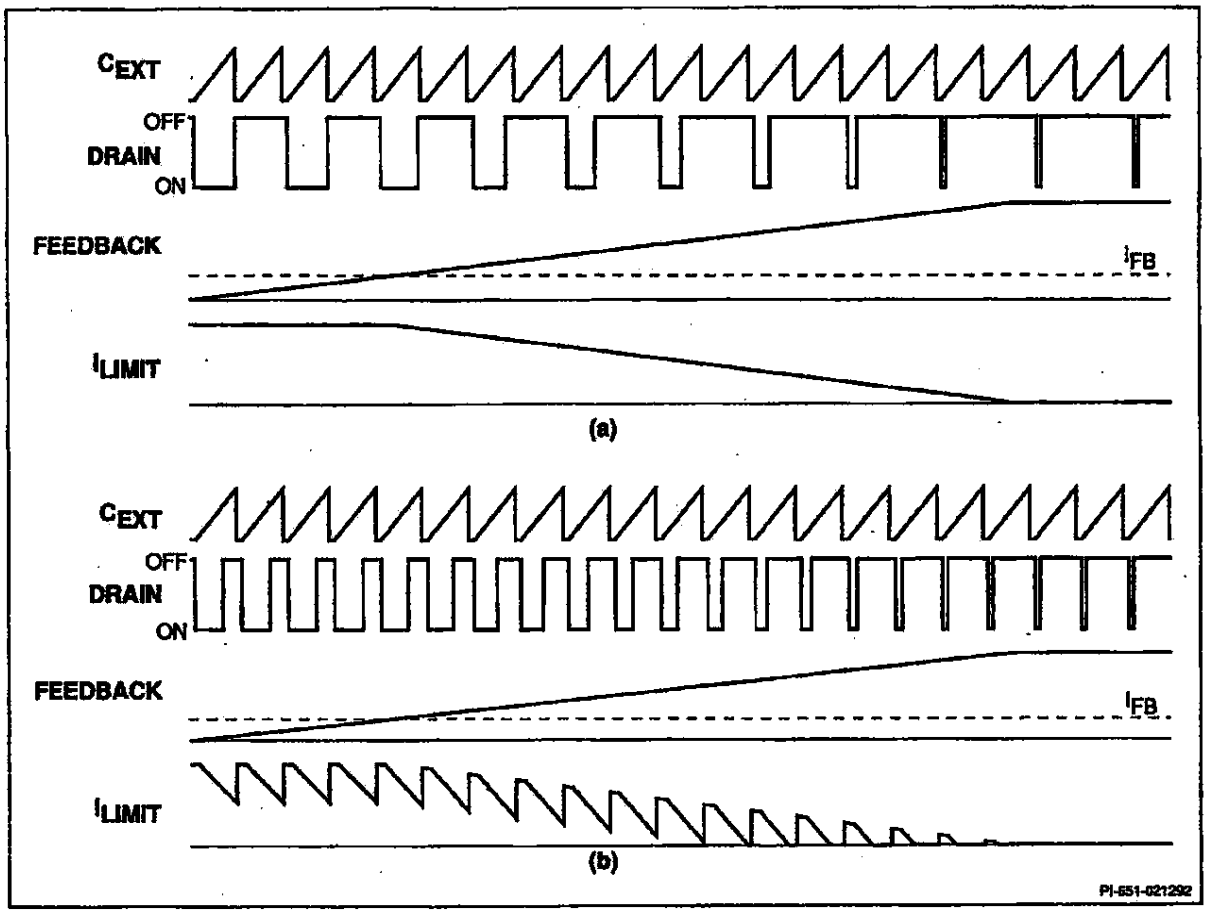


Figure 4. Typical Waveforms for (a)50% Maximum Duty Cycle Mode, and (b) 90% Maximum Duty Cycle Mode.

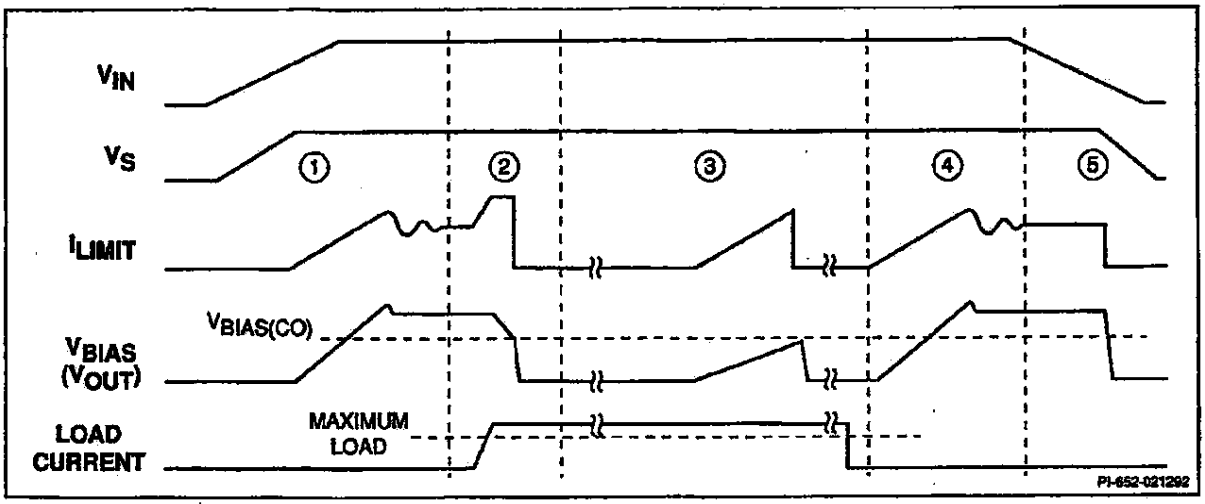


Figure 5. Typical Soft-start Waveforms. (1) Normal Power-up (2) Overload (3) Restart with Overload (4) Normal Restart (5) Normal Power-down.

30 W, Universal Off-line Power Supply

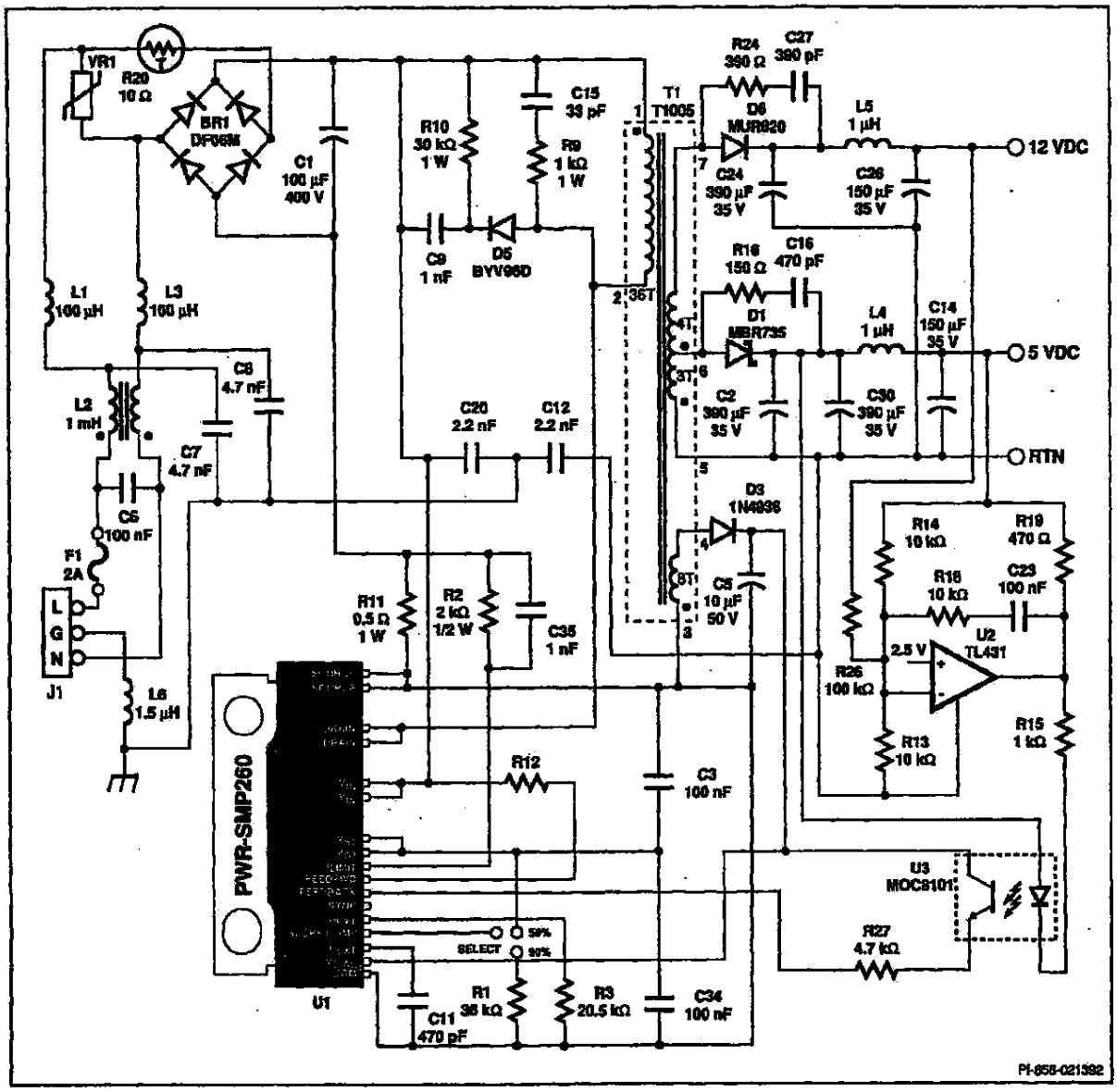


Figure 6. Schematic Diagram of a Single Output 30 W Supply Utilizing the PWR-SMP260.

General Circuit Operation

The flyback power supply circuit shown in Figure 6, when operated with the T1005 standard transformer (see DA-3), will produce a dual output (5 V/12 V), 30 watt power supply that will operate from 85 to 265 V(rms) AC input voltage. The turns ratio of the transformer and the output error amplifier resistor divider ratio R13 and R14 determine the output voltage. The use of the output error amplifier guarantees nearly ideal voltage regulation.

L1, L2, L3, C1, C6, C7, C8, C12, and C20 form an EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. L1, L3, C1, and C6 form a differential-mode noise filter. Differential mode noise is a result of the pulsating currents at the input of the switch mode power supply. C7, C8, C12, C20, L1, L2, and L3 form a common mode filter. The filter contains the capacitive displacement currents that flow between the primary windings of the transformer and the secondary output circuit.

D5, C9, and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damp the transformer leakage inductance ringing voltage.

C11 sets the frequency of operation. C3, C5, C34, and C35 are bypass capacitors. C3 supplies the pulse of current required to charge the gate of the output power transistor at turn on. D3 and C5 rectify and filter the bias winding voltage to form the V_{BIAS} supply. C34 is the analog bypass capacitor for V_{SI}. C35 is a noise suppression bypass capacitor.

R2 and R11 form the cycle-by-cycle current limit and current mode control circuitry. The value of R2 and the I_{LIMIT} current set the current sense comparator reference voltage. Thus the voltage drop and maximum power dissipation in the current sense resistor R11 can be adjusted as desired.

R1 sets the amount of slope compensation current flowing in the current mode control current (I_{LIMIT}). Typical values for R1 fall between 7 and 35 kΩ. When the slope compensation pin is connected to V_{SI}, the circuit is configured for 50% maximum duty cycle and R1 is no longer needed. R12 is the optional feedforward compensation resistor, which can be used for open loop compensation of current limit for changes in input voltage. R3 is a reference resistor that sets the current sources within the integrated circuit. The value of R3 must be as specified for data sheet performance specifications to be valid.

D1, C2, C14, C30, and L6 rectify and filter the 5 V output winding voltage. R19 and C16 damp the secondary leakage inductance ringing voltage caused by the stored charge of D1.

D6, C24, C26, and L5 rectify and filter the 12 V output winding voltage. R24 and C27 damp the secondary leakage inductance ringing voltage caused by the stored charge of D6.

U2, U3, R13, R14, R15, R18, R19, R26, and C23 form the output error amplifier circuit. R13 and R14 form the voltage divider that sets the output voltage. The value of R14 should be adjusted for changes in output voltage. The optical coupler must be connected to the input side of the output Pi-section filter to prevent high frequency oscillation of the control loop. R27 limits the AC current coupled from the V_{BIAS} supply through the optocoupler U3.

The current mode control function can be viewed as an adjustable current limit circuit. The output error amplifier circuit adjusts the current limit to maintain the desired output voltage. The output error amplifier decreases the output voltage and current of the switch mode regulator by increasing the optical coupler current. The optical coupler current decreases the current flowing from the I_{LIMIT} pin. This effectively decreases the current at which the current mode comparator will turn off the output transistor and decrease the output current and voltage.

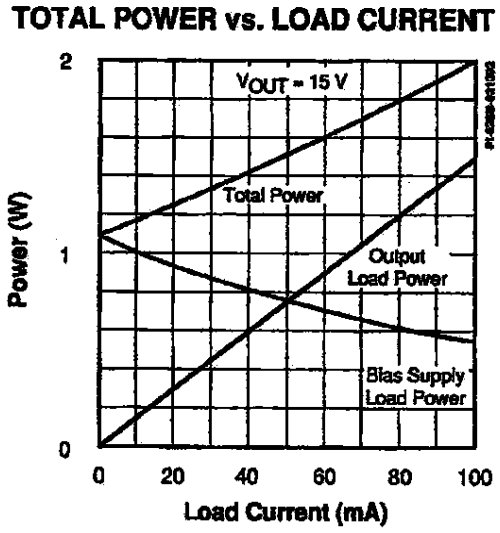


Figure 7. Minimum Load Transfer Characteristic.

General Circuit Operation (cont.)

The current mode comparator is inhibited during the blanking time so that any leading edge current pulse will not be misinterpreted and prematurely terminate a pulse. This has the side effect of providing a minimum pulse width for the output switch. A minimum width pulse will transfer an incremental amount of power to the output every time the power switch is turned on. This can be a problem during minimum load conditions.

The PWR-SMP260 has a minimum load regulator built in that monitors the onset of the minimum pulse width condition. The circuit monitors the summing junction current before slope compensation is added. When the summing junction current falls below 12% of full scale the shunt regulator starts to draw current from V_{BIAS}. The shunt regulator increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale.

When AC voltage is first applied to the input terminals of the power supply, the voltage on the line filter capacitor increases. The high-voltage linear regulator will regulate V_{S1} when V_{IN} is between 12 and 20 VDC. The V_{S1} undervoltage lockout circuit will hold the output switching transistor off and the last 8 bits of the soft- start counter chain reset until V_{S1} is in regulation, and the soft-start sequence begins. The peak switching current will increase as soft-start progresses. The soft-start time for a 120 kHz power supply is 34 ms, allowing the line filter capacitor two line cycles to fully charge. One cycle, 16.7 ms, is typically required to charge the line filter capacitor.

During the soft-start sequence, the counter chain runs and the five-bit digital to analog converter controls the maximum I_{LIMIT} current. The duty cycle of the output switch will increase as the peak switching current increases. When the output and V_{BIAS} voltages increase beyond the fault detection threshold to the regulation voltage, the output error amplifier will reduce the peak switch current. The output voltage will overshoot slightly and return to the desired voltage as the error amplifier frequency compensation capacitors stabilize to their steady-state bias voltage.

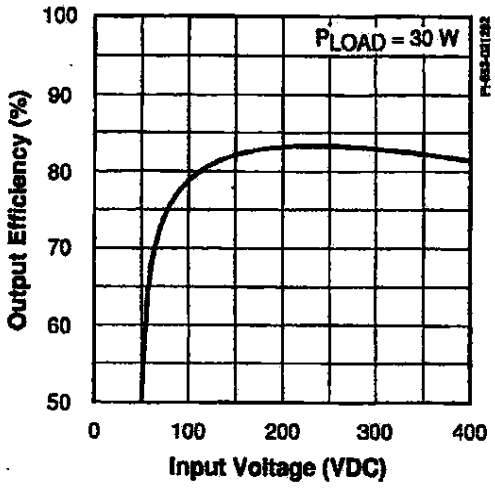
Figure 7 shows the minimum load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However this occurs when the dissipation in the switching MOSFET is very low and the package has excess thermal capacity.

The full featured soft-start will cycle the power supply on and off when an output fault condition is detected. The soft-start will cycle at 0.003% of the equivalent power supply output frequency. A fault condition exists until the V_{BIAS} voltage exceeds its threshold.

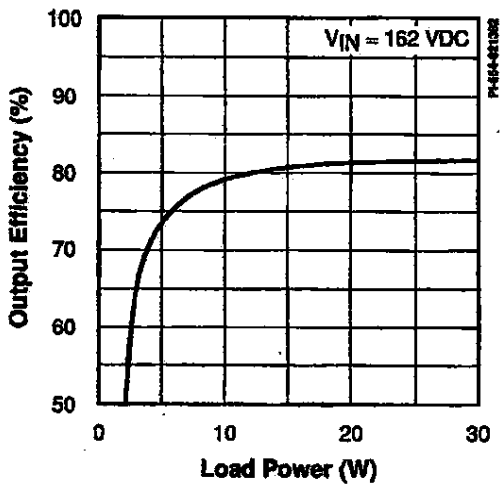
The circuit shown in Figure 6 is the schematic diagram of the PWR-EVAL7 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP260. Complete supply specifications are included, as will as instruction on how to modify the board for other output voltages and oscillator frequencies.

Typical Performance Characteristics (Figure 6 Power Supply)

EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



ABSOLUTE MAXIMUM RATINGS[1]

DRAIN Voltage ..... 700 V
V_{IN} Voltage ..... 500 V
V_{BIAS} Voltage ..... 35 V
V_{BIAS} Current ..... 300 mA
Feedback/Feedforward Current ..... 20 mA
Drain Current ..... 3 A
Storage Temperature ..... –65 to 125°C
Ambient Temperature ..... 0 to 70°C

Junction Temperature[2] ..... 150°C
Lead Temperature[3] ..... 260°C
Power Dissipation (T_A = 25°C) ..... 2.3 W
(T_A = 70°C) ..... 1.2 W
Thermal Impedance (θ_{JA}) ..... 41°C/W
(θ_{JC}) ..... 7.2°C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25°C
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Frequency Range	f_{OSC}		30		400	kHz
Initial Accuracy	Δf_{OSC}	SLOPE COMP Open	230	270	310	kHz
SYNC Pulse Width	t_{SYNC}	Output Synchronized to External Clock	0.1		1	µs
		Output OFF	10			
SYNC Bias Current	I_{SYNC}	Output Switching		170		µA
		Output OFF		35		
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	SLOPE COMP = V_S	0-45	0-50		%
		SLOPE COMP Open	0-90	0-95		
Summing Junction Current Gain	$A_{I(SJ)}$		1.9		2.2	
Summing Junction Gain-Bandwidth				1		MHz
Current Limit Threshold Voltage	V_{ILIMIT}		0		50	mV
Current Limit Reference Current	I_{REF}	SLOPE COMP = V_S, FEEDBACK, FEEDFORWARD Open		480		µA
Current Limit Delay Time	t_{ILIMIT}	V_{ILIMIT} = 150 mV		75		ns

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
PULSE WIDTH MODULATOR (cont.)						
SLOPE COMP Peak Voltage		SLOPE COMP to COM via 6.98 kΩ	1.7		1.8	V
SLOPE COMP Current Gain	$A_{I(SC)}$			0		dB
Leading Edge Blanking Time	t_{BLANK}		100		200	ns
Minimum Load Current Gain	$A_{I(ML)}$			75		dB
Minimum Load Gain-Bandwidth				30		kHz
Minimum Load Current Threshold	I_{LIMIT}			60		µA
Feedforward Voltage	V_{FF}			1.25		V
Feedback Bias Current	I_{FB}			480		µA
Feedback Input Impedance	$Z_{FEEDBACK}$	I_{FB} = 200 µA			1	kΩ
SOFT-START						
Ramp Period				4096		Cycles
Auto-restart Delay Period				28,672		Cycles
DAC Linearity			-1		1	lsb
CIRCUIT PROTECTION						
Thermal Shutdown Temperature			120	140		°C
Thermal Shutdown Hysteresis				45		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_j = 25°C			3	Ω
			T_j = 115°C			5	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		2	2.5		A
OFF-State Current	I_{DSS}	V_{DRAIN} = 560 V			10	100	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		700			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			280		pF
Output Stored Energy	E_{OSS}				2500		nJ
Rise Time	t_r					100	ns
Fall Time	t_f					100	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			20		500	V
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$			8	9	10	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected			5	TBD	mA
		V_{BIAS} > 10 V				0.2	
		Thermal Shutdown ON or SYNC = 0			0.8	1.2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback		10		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback			5	TBD	mA
V_S Source Voltage	V_S			5.0	5.8	6.5	V
V_S Source Current	I_S					200	µA

NOTES:

1. Applying >3.5 V to the I_{LIMIT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP260 is connected to a high-voltage power source when the test circuit is activated.

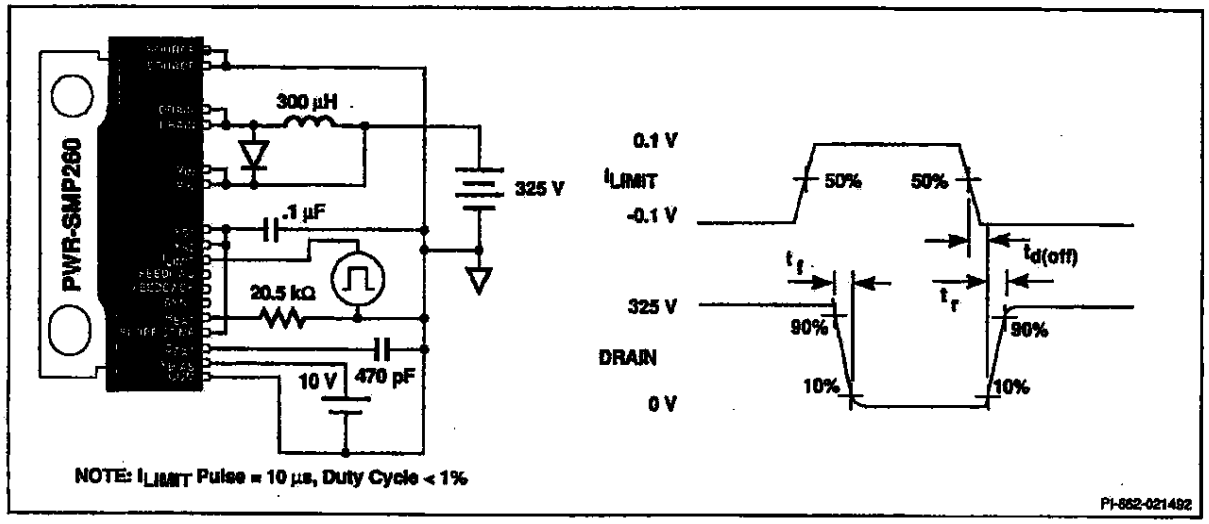
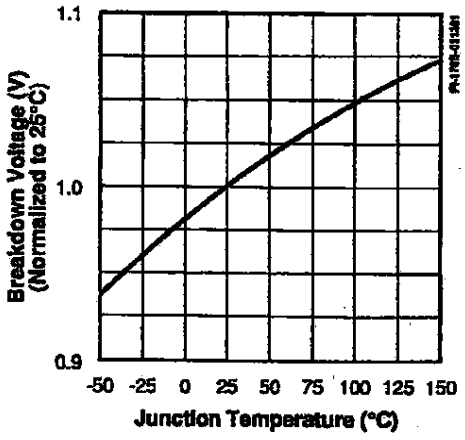
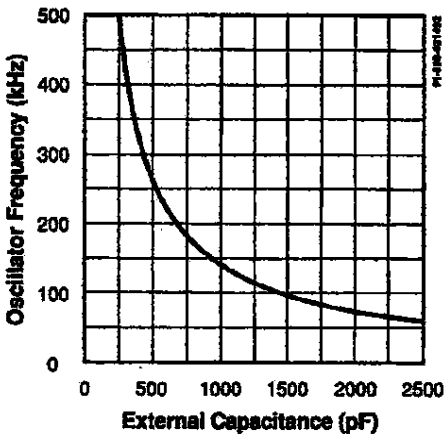


Figure 8. Switching Time Test Circuit.

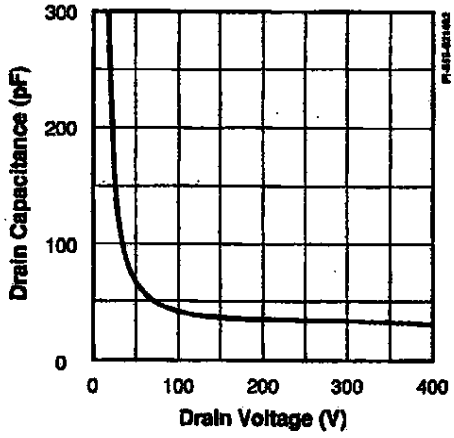
BREAKDOWN vs. TEMPERATURE



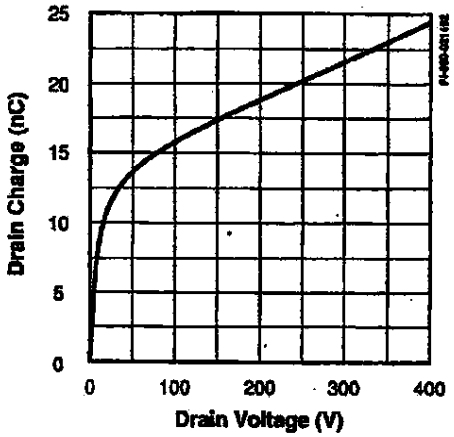
f_{PWM} vs. EXTERNAL CAPACITANCE



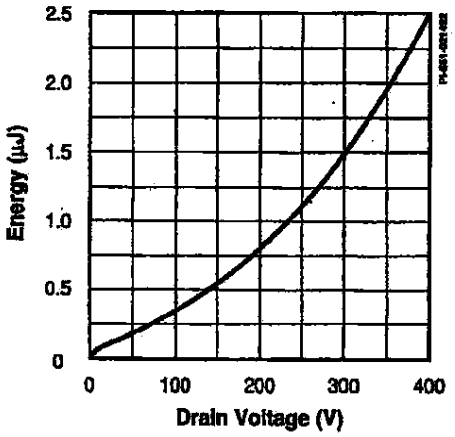
C_{OSS} vs. DRAIN VOLTAGE



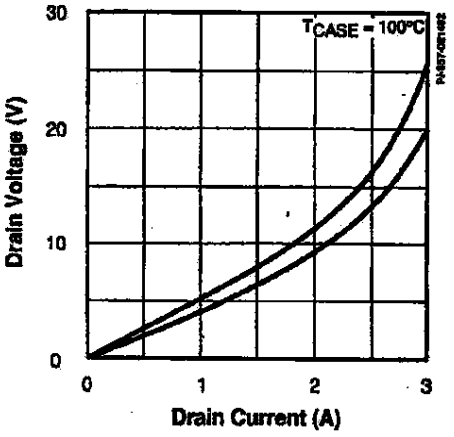
DRAIN CHARGE vs. DRAIN VOLTAGE



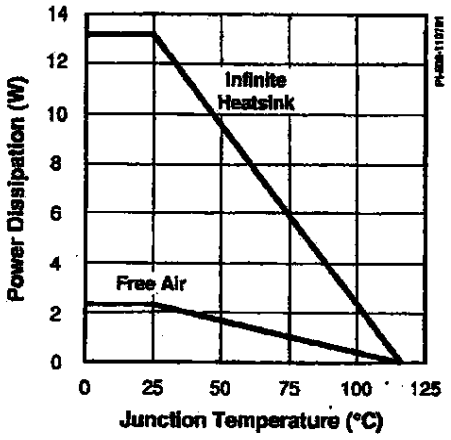
DRAIN CAPACITANCE ENERGY



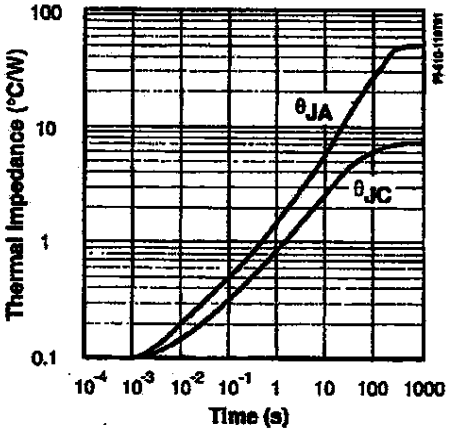
TRANSFER CHARACTERISTICS



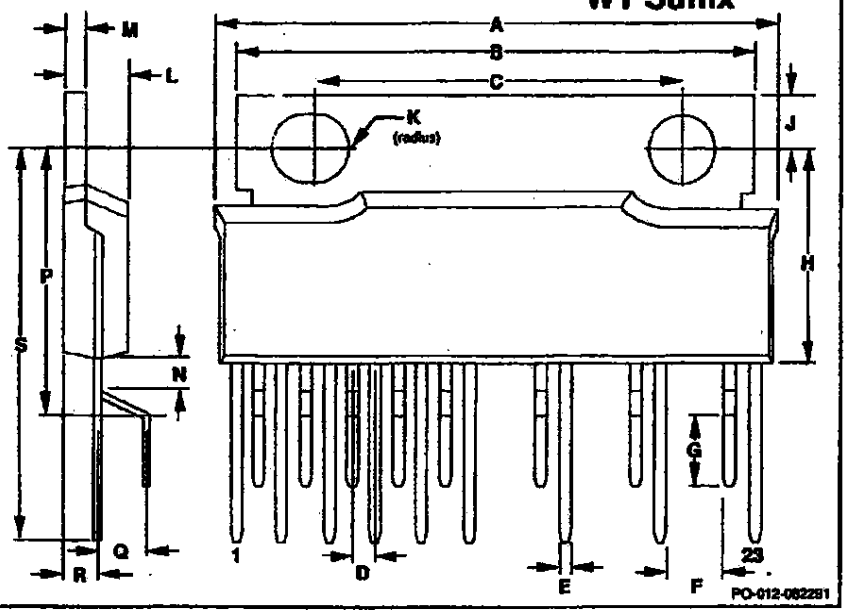
PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



DIM	INCHES	mm
A	1.157-1.161	29.40-30.00
B	1.091-1.114	27.70-28.30
C	.776-.799	19.70-20.30
D	.05	1.27
E	.0197-.0295	0.50-0.75
F	.125-.128	3.18-3.24
G	.177 TYP	4.5 TYP
H	.443-446	11.27-11.33
J	.110 TYP	2.8 TYP
K	.071 TYP	1.8 TYP
L	.126-.150	3.20-3.80
M	.041-.053	1.05-1.35
N	.041 TYP	1.03 TYP
P	.686 TYP	17.42 TYP
Q	.088-.112	2.24-2.84
R	.065-.077	1.65-1.95
S	.752 TYP	19.1 TYP



DX 123

PWR-SMP240

PWM Power Supply IC

85-265 VAC Input
Isolated, Regulated DC Output

POWER INTEGRATIONS, INC.

Product Highlights

Integrated Power Switch and CMOS Controller
- Output power up to 40 W from rectified 220/240 VAC input, 20 W from universal (85 to 265 VAC) input
- Feedforward control for constant-power battery charging
- External transformer provides isolation and selectable output voltages

High-speed Current-mode PWM Controller
- Leading edge current blanking
- Selectable maximum duty cycle - 50% or 90%
- Internal pre-regulator self-powers the IC on start-up
- Wide bias voltage range - 10-30 V
- Direct connection to optocoupler feedback
- Programmable slope compensation
- Low-current standby mode

Built-in Self-protection Circuits
- Full cycle soft-start - Linear ramp up of switching current
- Shutdown on fault with automatic restart
- Adjustable current limit
- Regulates from zero load to full load
- Undervoltage lockout
- Thermal shutdown

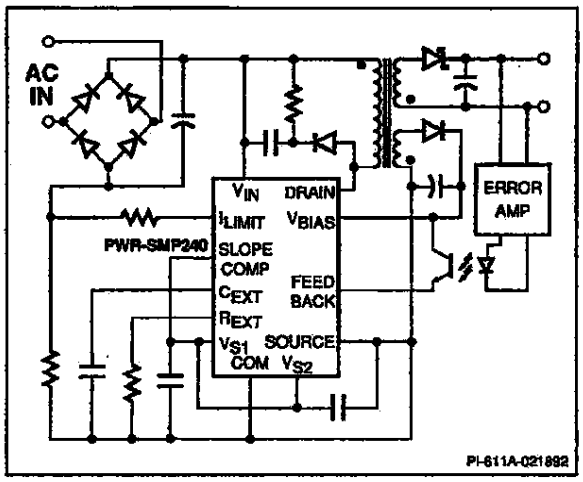


Figure 1. Typical Application

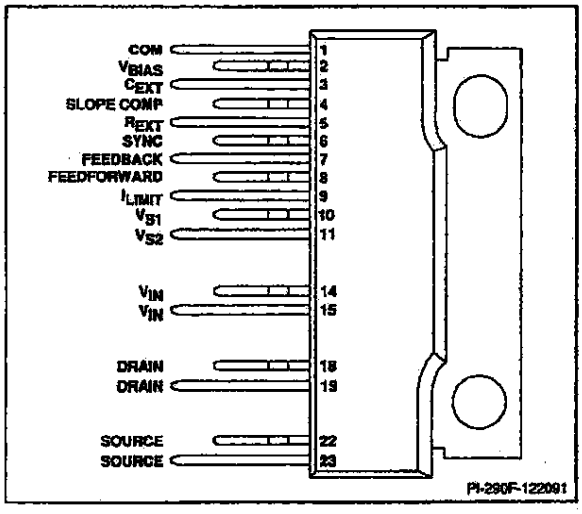


Figure 2. Pin Configuration

Description

The PWR-SMP240, intended for 220/240 VAC or universal off-line isolated power supply applications, combines a high voltage power MOSFET switch with a switchmode power system controller in a monolithic integrated circuit. Few external components are required to implement a low cost, isolated, off-line power supply. High frequency operation reduces total power supply size.

The current-mode PWM controller section of the PWR-SMP240 contains all the blocks required to drive and control the power stage: off-line pre-regulator, oscillator, bandgap reference, summing junction, PWM comparator, gate driver, soft-start, and circuit protection. The power MOSFET switch features include high voltage, low $R_{DS(ON)}$, low capacitance, and low gate threshold voltage.

The PWR-SMP240 is available in a plastic power SIP package. A surface mount power package version will be available in the second half of 1992.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-SMP240WTC	23-pin PWR SIP	0 to 70°C

411 Clyde Avenue
Mountain View, California, 94043
Phone: (415) 960-3572
Applications Hotline: (800) 552-3155
FAX: (800) 468-0809 In CA: (415) 940-1541

PRELIMINARY

February 1992

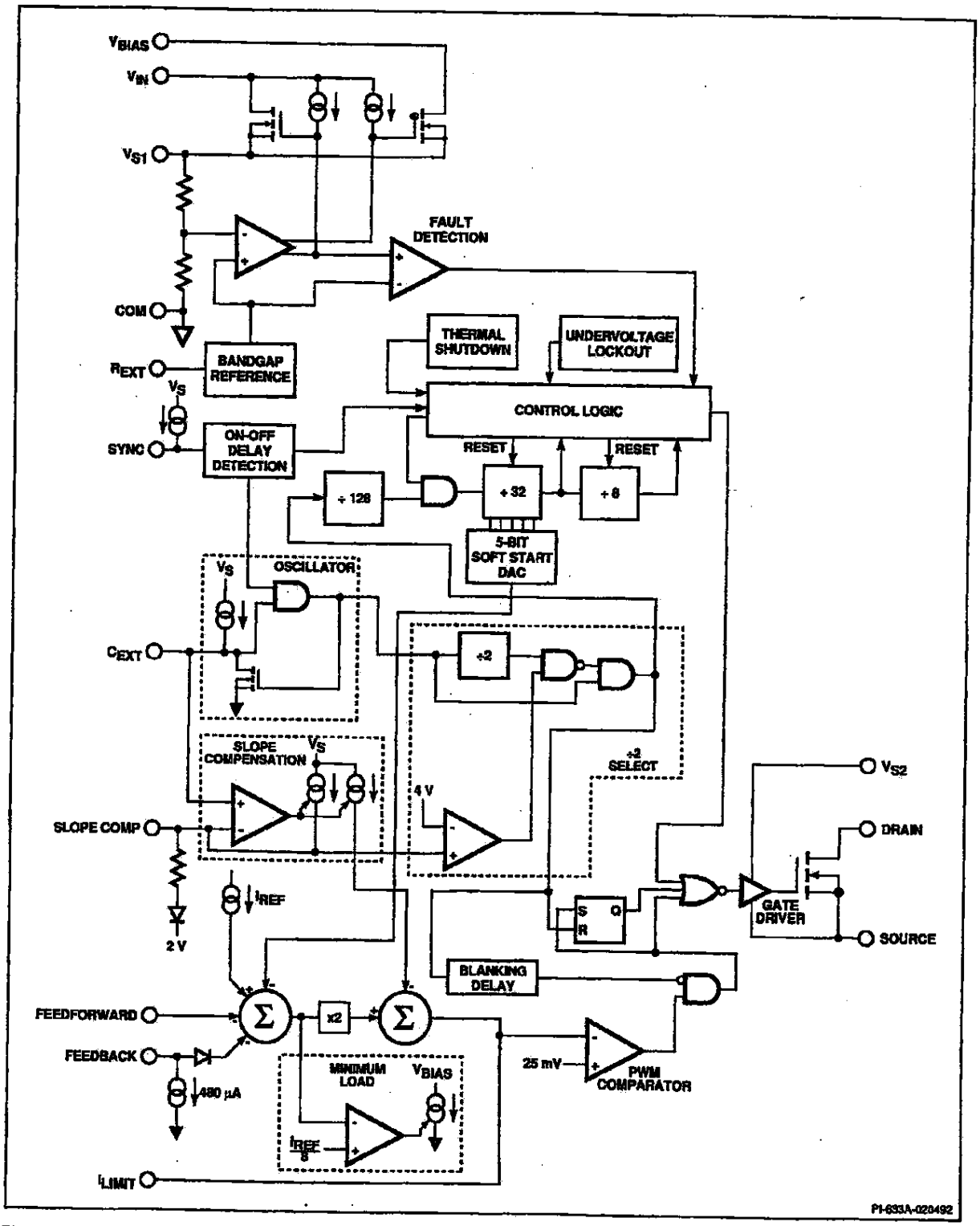


Figure 3. Functional Block Diagram of the PWR-SMP240.

Pin Functional Description

Pin 1:
COM is common reference point for all low-power and reference circuitry.

Pin 2:
V_{BIAS} is the bootstrap supply voltage proportional to the output voltage used to self-power the device once the supply is operating.

Pin 3:
C_{EXT} is used to set the oscillator frequency. Adding external capacitance between C_{EXT} and COM linearly decreases the PWM frequency.

Pin 4:
SLOPE COMP is used to select the amount of slope compensation to be injected into the summing junction in the maximum duty cycle mode. Connecting the pin to V_S selects 50% mode, and connction through a resistor to COM selects the 95% mode.

Pin 5:
A resistor placed between R_{EXT} and ANALOG COM sets the internal bias currents.

Pin 6:
SYNC is an active-low input with an internal pull-up used for synchronizing the oscillator. A continuous low level turns off the power supply output.

Pin 7:
FEEDBACK accepts current from an opto-coupler connected directly from V_{BIAS} which is controlled by an output-referenced error amplifier.

Pin 8:
FEEDFORWARD accepts current from an input voltage compensation resistor to automatically adjust the duty cycle for changes in input voltage.

Pin 9:
I_{LIMIT} is the output of the summing junction. Current flowing from this pin through a resistor will set the current comparator threshold.

Pin 10:
V_{S1} is the output of the internal V_{IN} and V_{BIAS} regulators. Connection to V_{S2} and an external bypass capacitor to COM is required for proper operation.

Pin 11:
The output gate drive circuit receives power via V_{S2}. Connection to V_{S1} and an external bypass capacitor to SOURCE is required for proper operation.

Pin 14, 15:
V_{IN} for connection to the high voltage pre-regulator used to self-power the device during start-up.

Pin 18, 19:
Open **DRAIN** of the output MOSFET.

Pin 22, 23:
The **SOURCE** is the high-current return for the output MOSFET.

PWR-SMP240 Functional Description

Off-line Linear and Bias Regulators
The off-line linear regulator powers the control circuits when the boot-strap bias voltage cannot. The off-line and bias linear regulator contains two high voltage MOSFETs, a gate bias current source, and an error amplifier. The error amplifier regulates V_S from either the off-line rectified voltage or the bias supply voltage, the bias supply voltage has preference to minimize power consumption.

The off-line linear regulator MOSFET dissipates significant amounts of power when supplying the bias current. When the V_{BIAS} voltage is greater than the V_{BIAS} threshold voltage the off-line linear regulator is cut off and internal bias current is supplied by the V_{BIAS} supply, decreasing the dissipation in the off-line regulator

V_{S1} is the output of the bias regulator and supplies power to all internal analog circuits. An external bypass capacitor connected between V_{S1} and SOURCE is required for filtering and noise reduction. V_{S2} is the power supply connection for the gate drive circuitry, and must be connected externally to V_{S1}. V_{S1} and V_{S2} are not internally connected.

Bandgap Reference
The reference voltage is generated by the temperature compensated bandgap reference and buffer. The voltage is used for setting thresholds for the current-mode regulator, soft-start, and over-temperature circuits. R_{EXT} is used by this circuit to provide precision current sources from the reference voltages.

PWR-SMP240 Functional Description (cont.)

Oscillator

The oscillator frequency is determined by the value of the external timing capacitor (C_{EXT}). An internal current source slowly charges C_{EXT} to a maximum. C_{EXT} is then rapidly discharged to its initial value.

When the oscillator frequency is being selected care should be taken to determine the selected maximum duty cycle. If the 50% maximum duty cycle option is selected the oscillator will need to operate at twice the output frequency. The slope compensation pin is used to select available maximum duty cycle.

The oscillator frequency can be synchronized to an external signal by applying a short synchronizing pulse to the SYNC pin. The free-running frequency of the oscillator must be set lower than the minimum synchronizing frequency.

The power supply can be turned off by holding the SYNC pin continuously low. When turned off, the power consumption of the control circuit is reduced to minimize standby power dissipation.

Pulse Width Modulator

The pulse width modulator combines the current sensing comparator, latch, and current summing junction functions.

The summing junction combines currents from the soft-start digital to analog converter current source, the slope compensation circuit, the feedback input and the feedforward input. The output of the summing junction is a current source. Current flowing from this pin through a resistor will set the current mode comparator threshold.

The current mode comparator sets the R-S flip-flop and turns off the output transistor when the voltage on the input to the current mode comparator falls to 25 mV. The current mode comparator input will be at 25 mV when the primary current reaches the desired peak value. The R-S flip-flop holds the output transistor off until the next cycle is ready to begin.

The feedback signal is diode coupled into the summing junction and a bias current source is provided so that an optical coupler can be DC biased without the addition of any external components. The feedback, feedforward, soft-start digital to analog converter and slope compensation current signals all reduce the current flowing from the output of the summing junction. The pulse width modulator adjusts the duty cycle to match the peak switch current with the scaled I_{LIMIT} current, as shown in Figure 4(a). The slope compensation current signal linearly reduces the instantaneous current flowing from the output of the summing junction over the cycle.

Slope compensation should be used when the maximum duty cycle exceeds 50%. The amount of slope compensation required is inversely related to the magnetizing current flowing in the output transistor. Figure 4(b) gives the relationships between the feedback current and the I_{LIMIT} current with an external slope compensation resistor. Refer to AN-11 for more detailed information on selecting slope compensation components.

Leading edge blanking of the current-mode comparator is provided by inhibiting the output of the comparator for a short time after the output transistor is turned on. The leading edge blanking time has been set so that ultra fast recovery rectifiers operating at their specified recovery times will not cause premature termination of the switching pulse.

The active minimum load circuit senses when the sum junction current is less than 12% of maximum sum junction current and increases the power consumption of the control circuit to maintain this minimum load power level. This will prevent the programmed current from falling to such a low level that the required pulse width would approach the blanking time.

Full Function Soft-Start

The soft-start circuit controls the pulse width modulator when the power supply is in a fault condition as demonstrated in Figure 5. During the time that the fault condition exists, the power supply will be enabled one eighth of the time. When the power supply is enabled, the I_{LIMIT} current ramps up from zero to the maximum value over 4096 cycles of the power supply. A 5-bit digital to analog converter current source controls the value of the Ilimit current and the output switch current. The controlled ramp up of the switch current limits the power stresses on the output diode rectifier and prevents the transformer from being driven into saturation.

The soft-start determines an output fault has occurred if the V_{BIAS} voltage is less than the V_{BIAS} threshold voltage after the soft-start ramp up time. During a fault condition, the output transistor is turned off for a period of 28,672 cycles of the power supply, after which the fault condition is tested by ramping up the switch current to full scale. If V_{BIAS} is not above the V_{BIAS} threshold voltage by the time full current is reached the fault condition is again detected and the switch is turned off.

Undervoltage Protection Circuit

The undervoltage protection circuit insures that the output transistor is off until the V_{SI} is regulated.

Overtemperature Protection Circuit

The overtemperature protection is provided by a precision analog circuit that turns the power switch off when the junction gets too hot (typically 140°C). The device will turn back on again when the junction has cooled past the hysteresis temperature level.

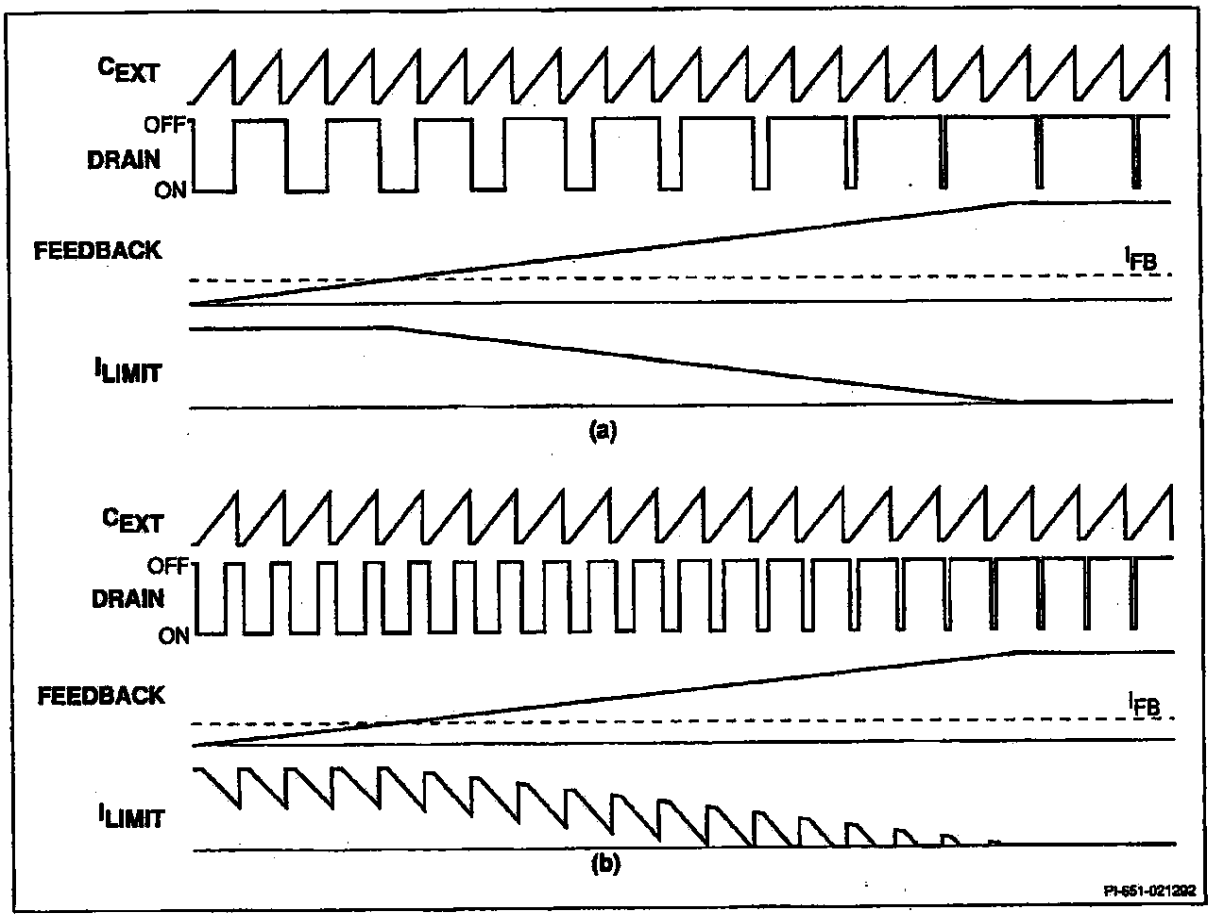


Figure 4. Typical Waveforms for (a)50% Maximum Duty Cycle Mode, and (b) 90% Maximum Duty Cycle Mode.

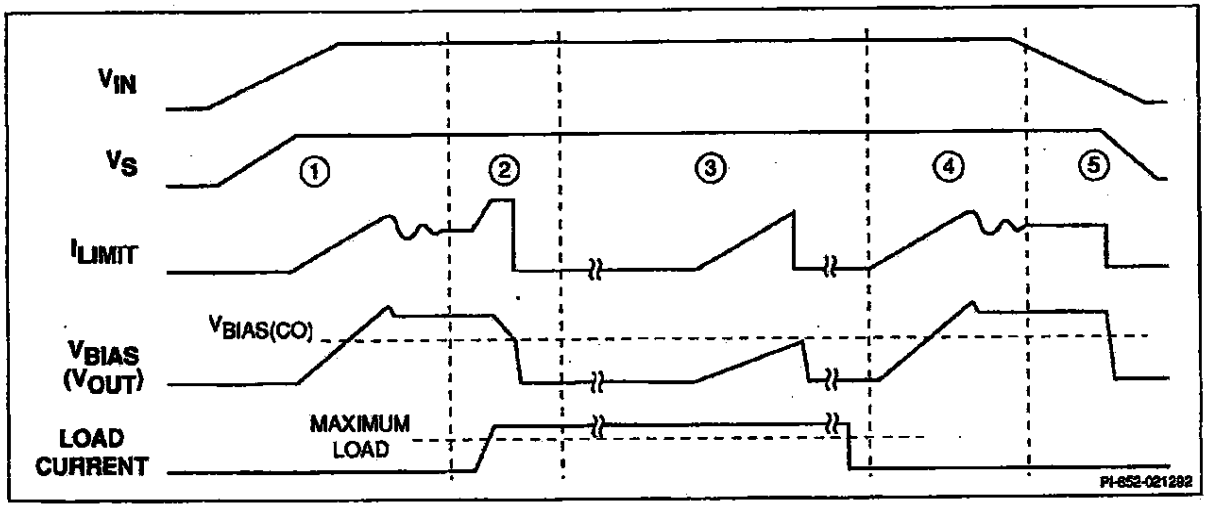


Figure 5. Typical Soft-start Waveforms. (1) Normal Power-up (2) Overload (3) Restart with Overload (4) Normal Restart (5) Normal Power-down.

20 W, Universal Off-line Power Supply

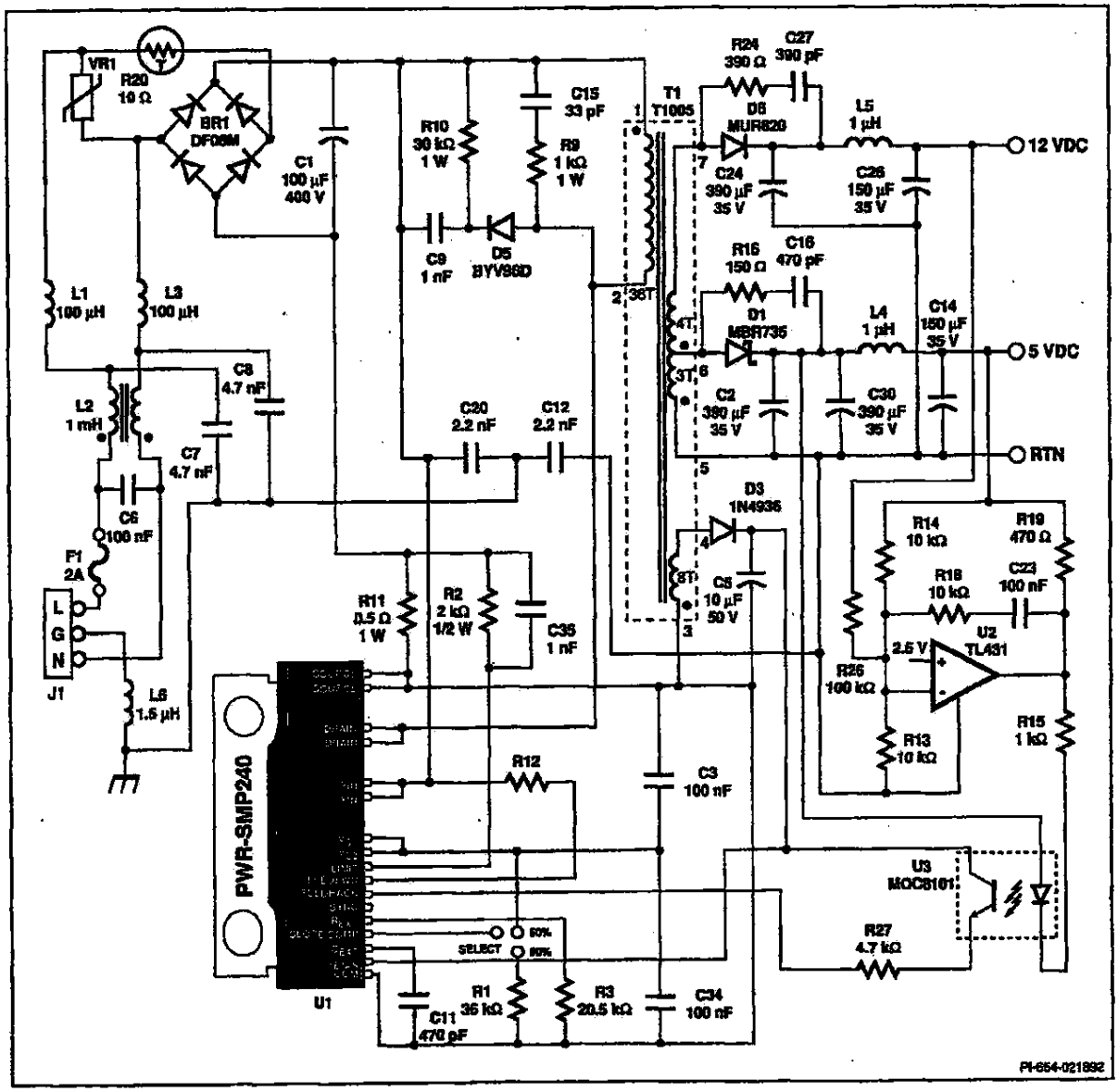


Figure 6. Schematic Diagram of a Single Output 20 W Supply Utilizing the PWR-SMP240.

General Circuit Operation

The flyback power supply circuit shown in Figure 6, when operated with the T1005 standard transformer (see DA-3), will produce a dual output (5 V/12 V), 20 watt power supply that will operate from 85 to 265 V(rms) AC input voltage. The turns ratio of the transformer and the output error amplifier resistor divider ratio R13 and R14 determine the output voltage. The use of the output error amplifier guarantees nearly ideal voltage regulation.

L1, L2, L3, C1, C6, C7, C8, C12, and C20 form an EMI filter. BR1 and C1 convert the AC input voltage to rectified DC voltage and provide the cycle-to-cycle hold-up time. L1, L3, C1, and C6 form a differential-mode noise filter. Differential mode noise is a result of the pulsating currents at the input of the switch mode power supply. C7, C8, C12, C20, L1, L2, and L3 form a common mode filter. The filter contains the capacitive displacement currents that flow between the primary windings of the transformer and the secondary output circuit.

D5, C9, and R10 make up a voltage clamping circuit to limit the peak voltage on the drain of the switching transistor. C15 and R9 damp the transformer leakage inductance ringing voltage.

C11 sets the frequency of operation. C3, C5, C34, and C35 are bypass capacitors. C3 supplies the pulse of current required to charge the gate of the output power transistor at turn on. D3 and C5 rectify and filter the bias winding voltage to form the V_{BIAS} supply. C34 is the analog bypass capacitor for V_{SI}. C35 is a noise suppression bypass capacitor.

R2 and R11 form the cycle-by-cycle current limit and current mode control circuitry. The value of R2 and the I_{LIMIT} current set the current sense comparator reference voltage. Thus the voltage drop and maximum power dissipation in the current sense resistor R11 can be adjusted as desired.

R1 sets the amount of slope compensation current flowing in the current mode control current (I_{LIMIT}). Typical values for R1 fall between 7 and 35 kΩ. When the slope compensation pin is connected to V_{SI}, the circuit is configured for 50% maximum duty cycle and R1 is no longer needed. R12 is the optional feedforward compensation resistor, which can be used for open loop compensation of current limit for changes in input voltage. R3 is a reference resistor that sets the current sources within the integrated circuit. The value of R3 must be as specified for data sheet performance specifications to be valid.

D1, C2, C14, C30, and L6 rectify and filter the 5 V output winding voltage. R19 and C16 damp the secondary leakage inductance ringing voltage caused by the stored charge of D1.

D6, C24, C26, and L5 rectify and filter the 12 V output winding voltage. R24 and C27 damp the secondary leakage inductance ringing voltage caused by the stored charge of D6.

U2, U3, R13, R14, R15, R18, R19, R26, and C23 form the output error amplifier circuit. R13 and R14 form the voltage divider that sets the output voltage. The value of R14 should be adjusted for changes in output voltage. The optical coupler must be connected to the input side of the output Pi-section filter to prevent high frequency oscillation of the control loop. R27 limits the AC current coupled from the V_{BIAS} supply through the optocoupler U3.

The current-mode control function can be viewed as an adjustable current limit circuit. The output error amplifier circuit adjusts the current limit to maintain the desired output voltage. The output error amplifier decreases the output voltage and current of the switch mode regulator by increasing the optical coupler current. The optical coupler current decreases the current flowing from the I_{LIMIT} pin. This effectively decreases the current at which the current mode comparator will turn off the output transistor and decrease the output current and voltage.

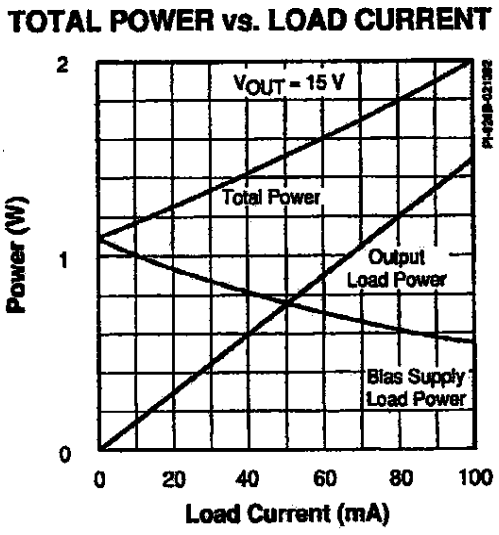


Figure 7. Minimum Load Transfer Characteristic.

General Circuit Operation (cont.)

The current mode comparator is inhibited during the blanking time so that any leading edge current pulse will not be misinterpreted and prematurely terminate a pulse. This has the side effect of providing a minimum pulse width for the output switch. A minimum width pulse will transfer an incremental amount of power to the output every time the power switch is turned on. This can be a problem during minimum load conditions.

The PWR-SMP240 has a minimum load regulator built in that monitors the onset of the minimum pulse width condition. The circuit monitors the summing junction current before slope compensation is added. When the summing junction current falls below 12% of full scale the shunt regulator starts to draw current from V_{BIAS}. The shunt regulator increases the load on the bootstrap bias supply until the summing junction current returns to 12% of full scale.

When AC voltage is first applied to the input terminals of the power supply, the voltage on the line filter capacitor increases. The high-voltage linear regulator will regulate V_{SI} when V_{IN} is between 12 and 20 VDC. The V_{SI} undervoltage lockout circuit will hold the output switching transistor off and the last 8 bits of the soft- start counter chain reset until V_{SI} is in regulation, and the soft-start sequence begins. The peak switching current will increase as soft-start progresses. The soft-start time for a 120 kHz power supply is 34 ms, allowing the line filter capacitor two line cycles to fully charge. One cycle, 16.7 ms, is typically required to charge the line filter capacitor.

During the soft-start sequence, the counter chain runs and the five-bit digital to analog converter controls the maximum I_{LIMIT} current. The duty cycle of the output switch will increase as the peak switching current increases. When the output and V_{BIAS} voltages increase beyond the fault detection threshold to the regulation voltage, the output error amplifier will reduce the peak switch current. The output voltage will overshoot slightly and return to the desired voltage as the error amplifier frequency compensation capacitors stabilize to their steady-state bias voltage.

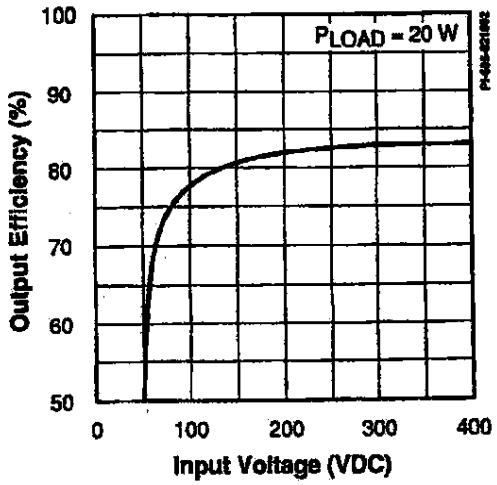
Figure 7 shows the minimum load transfer effect. As the external load drops below the minimum, the bias load increases to compensate and the load on the switching regulator is relatively constant. The power dissipation in the integrated circuit increases when the minimum load circuit is active. However this occurs when the dissipation in the switching MOSFET is very low and the package has excess thermal capacity.

The full featured soft-start will cycle the power supply on and off when an output fault condition is detected. The soft-start will cycle at 0.003% of the equivalent power supply output frequency. A fault condition exists until the V_{BIAS} voltage exceeds its threshold.

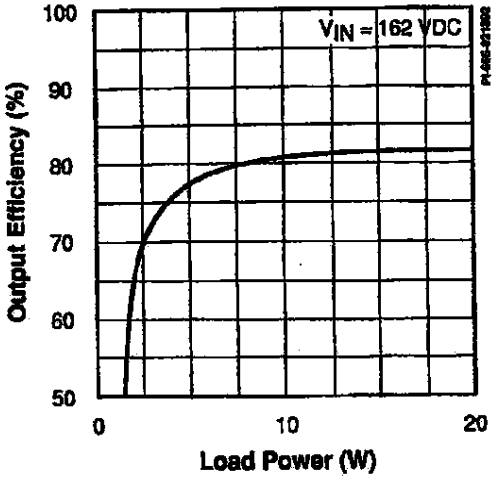
The circuit shown in Figure 6 is the schematic diagram of the PWR-EVAL8 evaluation board. This completely assembled and tested board can be ordered directly from Power Integrations, Inc. for evaluation of the PWR-SMP240. Complete supply specifications are included, as will as instruction on how to modify the board for other output voltages and oscillator frequencies.

Typical Performance Characteristics (Figure 6 Power Supply)

EFFICIENCY vs. INPUT VOLTAGE



EFFICIENCY vs. OUTPUT POWER



ABSOLUTE MAXIMUM RATINGS[1]

DRAIN Voltage ..... 700 V
V_{IN} Voltage ..... 500 V
V_{BIAS} Voltage ..... 35 V
V_{BIAS} Current ..... 300 mA
Feedback/Feedforward Current ..... 20 mA
Drain Current ..... 2 A
Storage Temperature ..... –65 to 125°C
Ambient Temperature ..... 0 to 70°C

Junction Temperature[2] ..... 150°C
Lead Temperature[3] ..... 260°C
Power Dissipation (T_A = 25°C) ..... 2.3 W
(T_A = 70°C) ..... 1.2 W
Thermal Impedance (θ_{JA}) ..... 41°C/W
(θ_{JC}) ..... 7.2°C/W

1. Unless noted, all voltages referenced to SOURCE, T_A = 25°C
2. Normally limited by internal circuitry.
3. 1/16" from case for 5 seconds.

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} =325 V, C_{EXT} = 470 pF R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
OSCILLATOR						
Frequency Range	f_{OSC}		30		400	kHz
Initial Accuracy	Δf_{OSC}	SLOPE COMP Open	230	270	310	kHz
SYNC Pulse Width	t_{SYNC}	Output Synchronized to External Clock	0.1		1	µs
		Output OFF	10			
SYNC Bias Current	I_{SYNC}	Output Switching		170		µA
		Output OFF		35		
PULSE WIDTH MODULATOR						
Duty Cycle Range	DC	SLOPE COMP = V_S	0-45	0-50		%
		SLOPE COMP Open	0-90	0-95		
Summing Junction Current Gain	$A_{I(SJ)}$		1.9		2.2	
Summing Junction Gain-Bandwidth				1		MHz
Current Limit Threshold Voltage	V_{ILIMIT}		0		50	mV
Current Limit Reference Current	I_{REF}	SLOPE COMP = V_S FEEDBACK, FEEDFORWARD Open		480		µA
Current Limit Delay Time	t_{ILIMIT}	V_{ILIMIT} = 150 mV		75		ns

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C	Test Limits MIN	TYP	MAX	Units
PULSE WIDTH MODULATOR (cont.)						
SLOPE COMP Peak Voltage		SLOPE COMP to COM via 6.98 kΩ	1.7		1.8	V
SLOPE COMP Current Gain	$A_{I(SC)}$			0		dB
Leading Edge Blanking Time	t_{BLANK}		100		200	ns
Minimum Load Current Gain	$A_{I(ML)}$			75		dB
Minimum Load Gain-Bandwidth				30		kHz
Minimum Load Current Threshold	I_{LIMIT}			60		µA
Feedforward Voltage	V_{FF}			1.25		V
Feedback Bias Current	I_{FB}			480		µA
Feedback Input Impedance	$Z_{FEEDBACK}$	I_{FB} = 200 µA			1	kΩ
SOFT-START						
Ramp Period				4096		Cycles
Auto-restart Delay Period				28,672		Cycles
DAC Linearity			-1		1	lsb
CIRCUIT PROTECTION						
Thermal Shutdown Temperature			120	140		°C
Thermal Shutdown Hysteresis				45		°C

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{IN} = 325 V, C_{EXT} = 470 pF, R_{EXT} = 20.5 kΩ, T_A = 0 to 70°C		Test Limits MIN	Test Limits TYP	Test Limits MAX	Units
OUTPUT							
ON-State Resistance	$R_{DS(ON)}$	I_D = 100 mA	T_J = 25°C			5	Ω
			T_J = 115°C			8.5	
ON-State Current	$I_{D(ON)}$	V_{DS} = 10 V		1.2	1.5		A
OFF-State Current	I_{DSS}	V_{DRAIN} = 560 V			10	100	µA
Breakdown Voltage	BV_{DSS}	I_{DRAIN} = 100 µA, T_A = 25°C		700			V
Output Capacitance	C_{OSS}	V_{DRAIN} = 25 V, f = 1 MHz			200		pF
Output Stored Energy	E_{OSS}				1500		nJ
Rise Time	t_r					100	ns
Fall Time	t_f					100	ns
SUPPLY							
Pre-regulator Voltage	V_{IN}			20		500	V
Pre-regulator Cutoff Voltage	$V_{BIAS(CO)}$			8	9	10	V
Off-line Supply Current	I_{IN}	V_{BIAS} not connected			5	TBD	mA
		V_{BIAS} > 10 V				0.2	
		Thermal Shutdown ON or SYNC = 0			0.8	1.2	
V_{BIAS} Supply Voltage	V_{BIAS}	V_{BIAS} externally supplied via feedback		10		30	V
V_{BIAS} Supply Current	I_{BIAS}	V_{BIAS} externally supplied via feedback			5	TBD	mA
V_S Source Voltage	V_S			5.0	5.8	6.5	V
V_S Source Current	I_S					200	µA

NOTES:

1. Applying >3.5 V to the I_{LIMIT} pin activates an internal test circuit that turns on the output switch continuously. Destruction of the part can occur if the output of the PWR-SMP240 is connected to a high-voltage power source when the test circuit is activated.

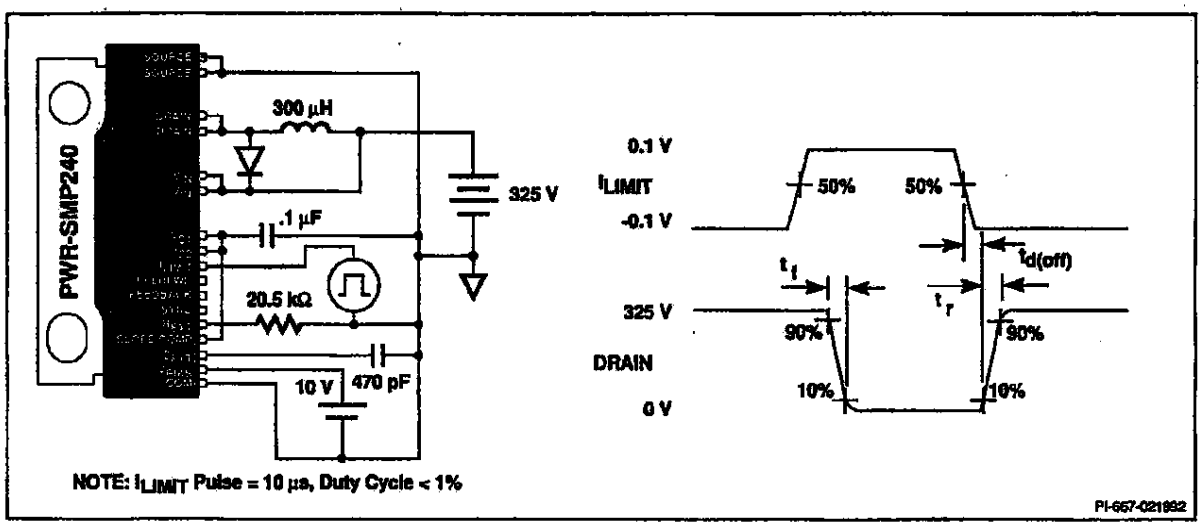
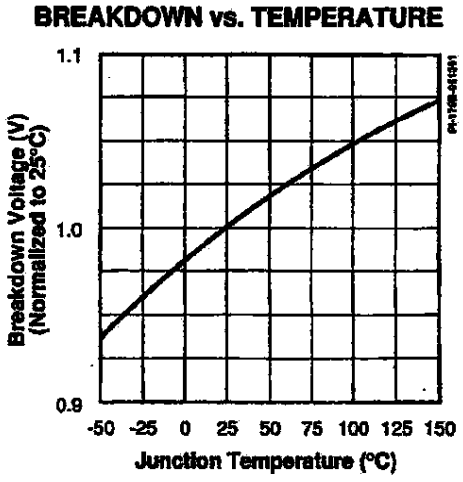
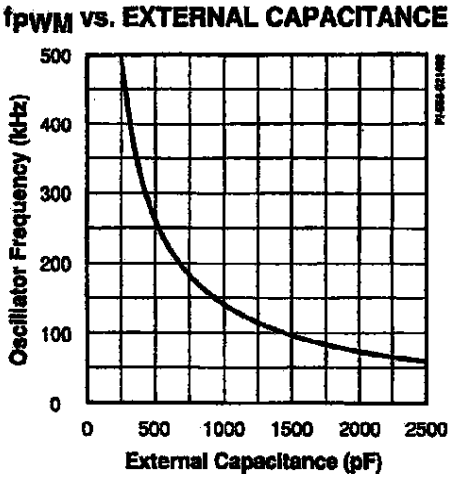
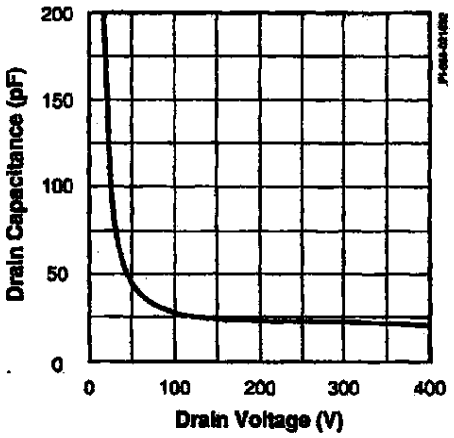


Figure 8. Switching Time Test Circuit.

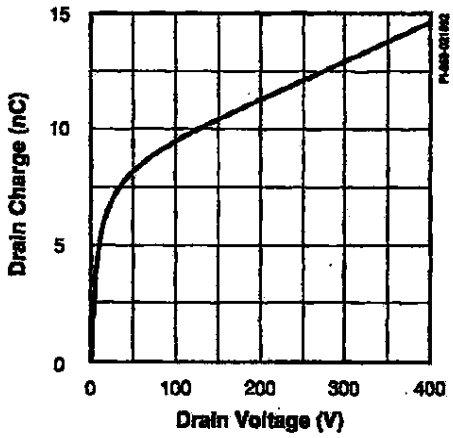




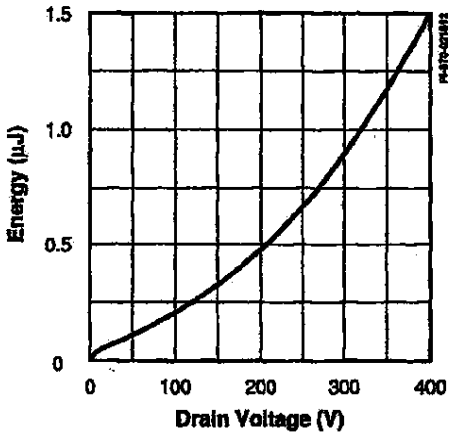
C_{OSS} vs. DRAIN VOLTAGE



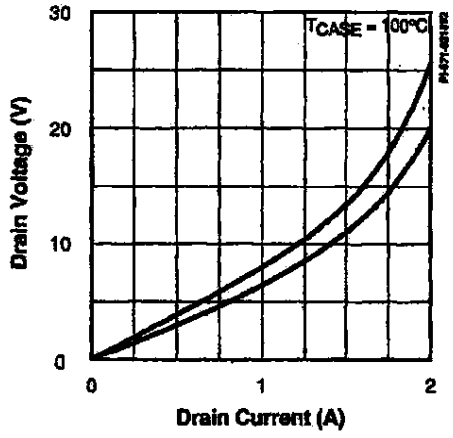
DRAIN CHARGE vs. DRAIN VOLTAGE



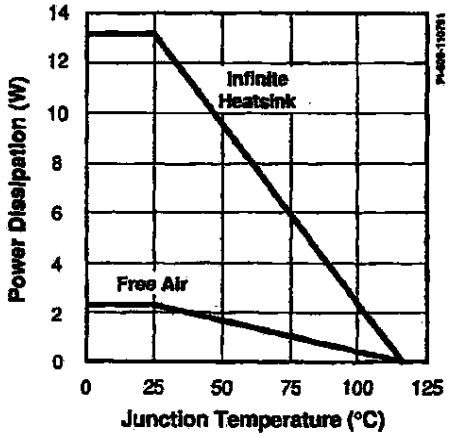
DRAIN CAPACITANCE ENERGY



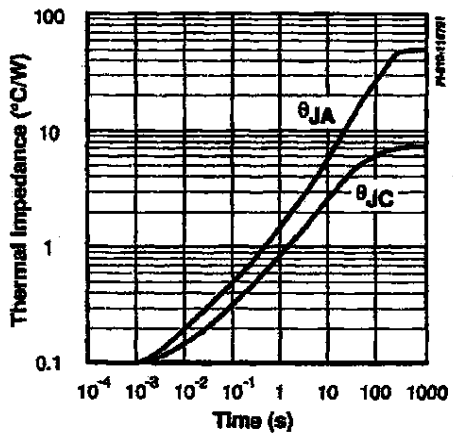
TRANSFER CHARACTERISTICS



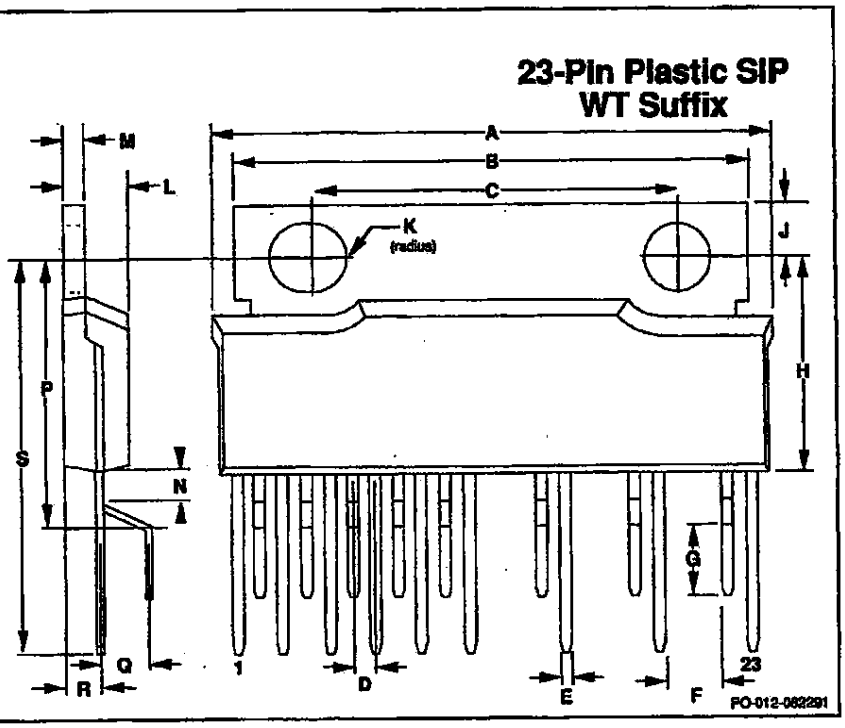
PACKAGE POWER DERATING



TRANSIENT THERMAL IMPEDANCE



DIM	Inches	mm
A	1.157-1.181	29.40-30.00
B	1.091-1.114	27.70-28.30
C	.776-.799	19.70-20.30
D	.05	1.27
E	.0197-.0295	0.50-0.75
F	.125-.128	3.18-3.24
G	.177 TYP	4.5 TYP
H	.443-446	11.27-11.33
J	.110 TYP	2.8 TYP
K	.071 TYP	1.8 TYP
L	.126-.150	3.20-3.80
M	.041-.053	1.05-1.35
N	.041 TYP	1.03 TYP
P	.686 TYP	17.42 TYP
Q	.088-.112	2.24-2.84
R	.065-.077	1.65-1.95
S	.752 TYP	19.1 TYP



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US005146298A

United States Patent [19]

Eklund

[11] Patent Number: 5,146,298

[45] Date of Patent: Sep. 8, 1992

[54] **DEVICE WHICH FUNCTIONS AS A LATERAL DOUBLE-DIFFUSED INSULATED GATE FIELD EFFECT TRANSISTOR OR AS A BIPOLAR TRANSISTOR**

[76] Inventor: Klas H. Eklund, 103 Los Patios, Los Gatos, Calif. 95030

[21] Appl. No.: 747,657

[22] Filed: Aug. 16, 1991

[51] Int. Cl.[5] H01L 29/80; H01L 29/10; H01L 29/72; H01L 27/04

[52] U.S. Cl. 357/22; 357/23.4; 357/34; 357/48

[58] Field of Search 357/22, 23.4, 34, 48

[56] References Cited

U.S. PATENT DOCUMENTS

4,626,879 12/1982 Colak 357/23.4
4,811,075 3/1989 Eklund 357/46

OTHER PUBLICATIONS

Sel Colak, "Effects of Drift Region Parameters on the Static Properties of Power LDMOS", IEEE Transactions on Electron Devices, vol. ED-28, No. 12, pp. 1455-1466 (Dec. 1981).

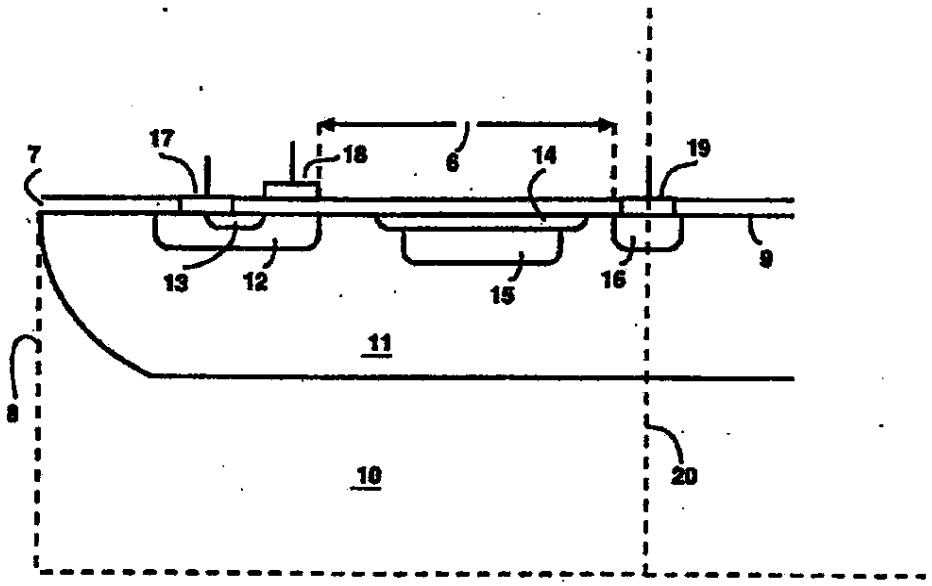
A. W. Ludikhuize, *High-Voltage DMOS and PMOS in Analog IC's*, IEDM, pp. 81-84 (1982).

Primary Examiner—Mark V. Prenty
Attorney, Agent, or Firm—Douglas L. Weller

[57] ABSTRACT

An insulated gate field effect transistor with an extended drain region is presented. The extended drain region includes a single-sided JFET and a double-sided JFET connected in parallel. The insulated gate field effect transistor is built on a substrate of first conductivity type. A pocket of semiconductor material of second conductivity type is within the substrate adjoining a surface of the substrate. A body region of semiconductor material of the first conductivity type is within the pocket adjoining the surface of the substrate. Also, a source region of semiconductor material of the second conductivity type is within the body region adjoining the surface of the substrate. A drain contact region of semiconductor material of the second conductivity type is also within the pocket of semiconductor material adjoining the surface of the substrate. A first intermediate region of semiconductor material of the first conductivity type is within the pocket of semiconductor material between the body region and the drain contact region. The first intermediate region adjoins the surface of the substrate. Also, a second intermediate region of semiconductor material of second conductivity type is within the pocket of semiconductor material between the body region and the drain contact region. The second intermediate region also adjoins the surface of the substrate. A portion of the second intermediate region extends between the first intermediate region and the surface of the substrate.

22 Claims, 5 Drawing Sheets



Case No. 04-1371-JJF
DEFT Exhibit No. DX 192
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Signature _____

PIF 56893

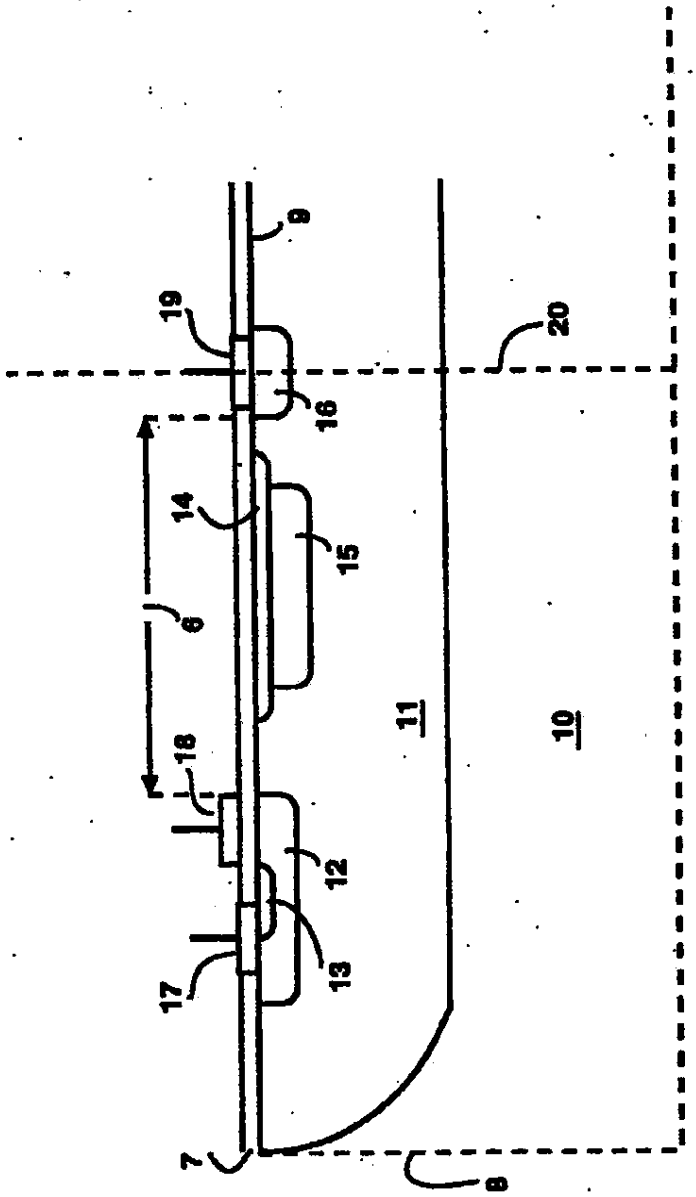

FIG. 1

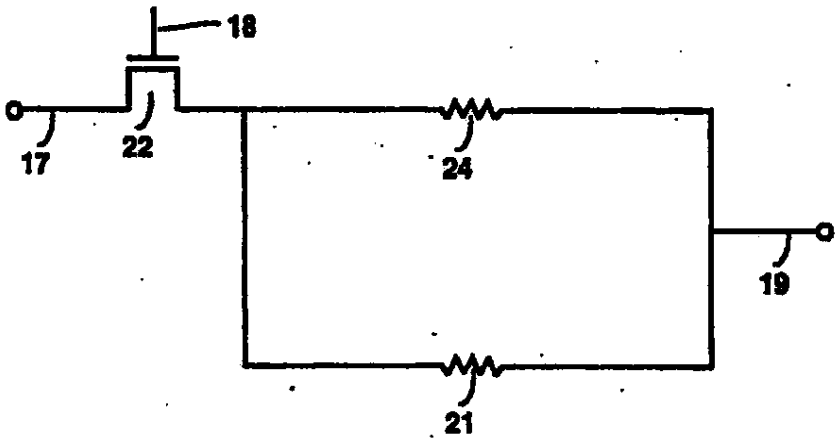

FIG. 2

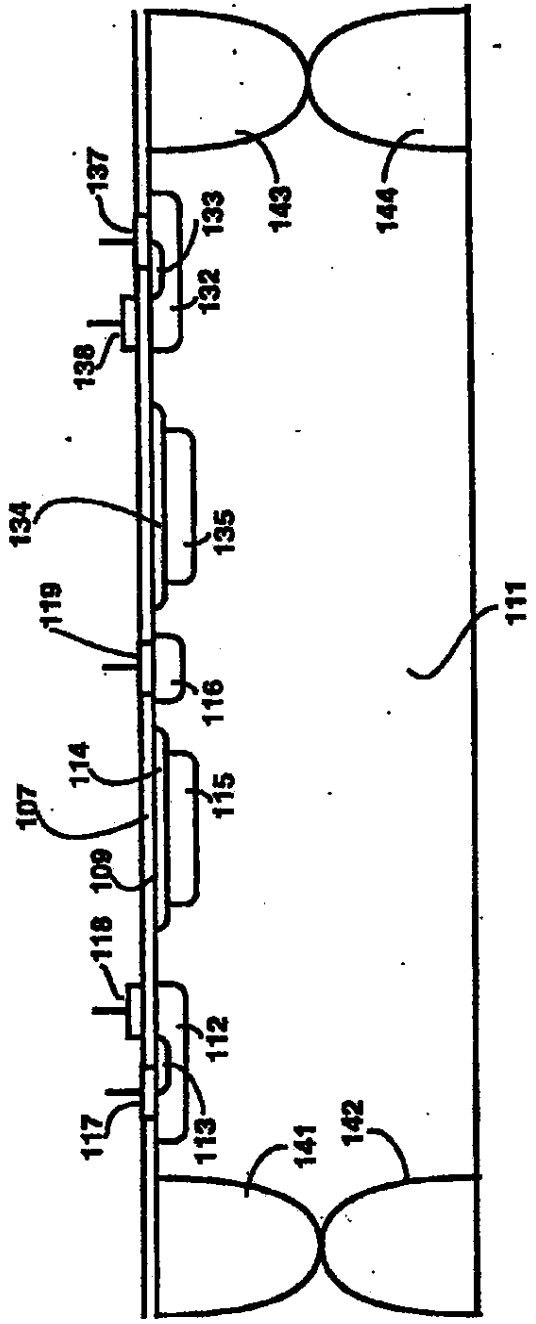
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FIG. 3

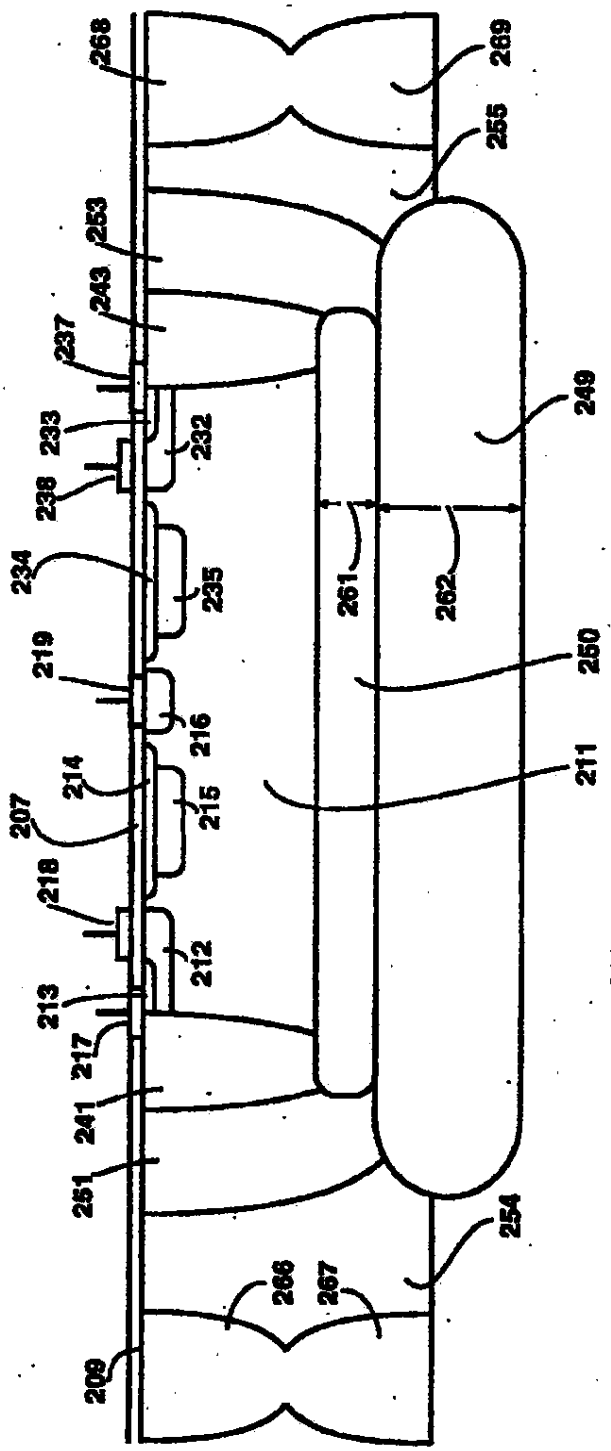
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FIG. 4

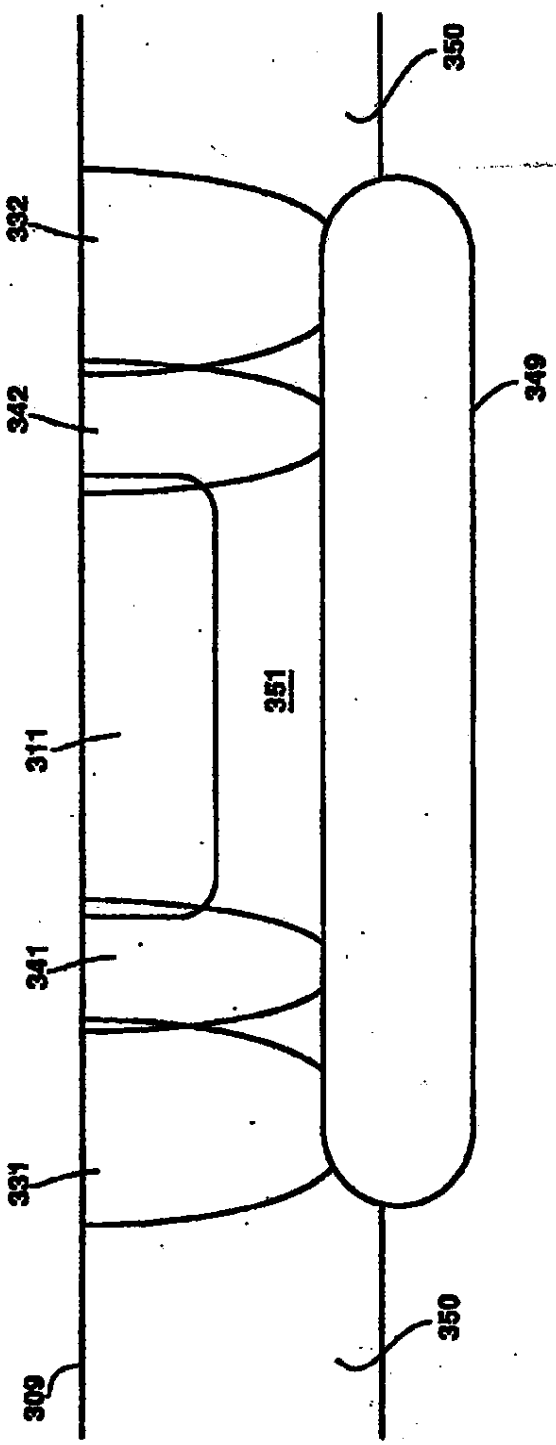

FIG. 5

DEVICE WHICH FUNCTIONS AS A LATERAL DOUBLE-DIFFUSED INSULATED GATE FIELD EFFECT TRANSISTOR OR AS A BIPOLAR TRANSISTOR

BACKGROUND

The present invention concerns a lateral double-diffused insulated gate field effect transistor where the extended drain region is a parallel combination of a single-sided junction field effect transistor (JFET) and a double-sided JFET. The present invention also relates to the construction of a bipolar transistor with an extended collector region. The present invention additionally relates generally to how metal-oxide-silicon (MOS) and/or a bipolar transistors can be effectively shielded from a substrate in a classic junction isolated technology.

Thin layer (resurfed) lateral double diffused metal oxide silicon (D-MOS) transistors have been shown to be an efficient means to integrate high voltage devices in the same die as low voltage control functions. See, for example, Sel Colak *Effects of Drift Region Parameters on the Static Properties of Power LDMOS*, IEE Transactions on Electron Devices, VOL. ED-28, No. 12, pp. 1455–1466 (December 1981). This reference describes a device which can be considered a series combination of a D-MOS transistor and a single-sided JFET. The single-sided JFET functions as a pinch resistor. The JFET is commonly a thin n-type epitaxial layer deposited on top of a p-type substrate.

In order to improve thin layer lateral D-MOS transistors as a source follower and further reduce resistance when the device is "on", a surface layer of p-type doping has been added. The modified device can be considered a D-MOS transistor in series with a double-sided JFET. See for example, A. W. Ludikhuize, *High-Voltage DMOS and PMOS in Analog IC's*, IEDM, pp. 81–84 (1982).

An efficient and simplistic way to incorporate a thin layer lateral high voltage MOS transistor which constitutes a series combination of a normal MOS transistor (not D-MOS) and a double-sided JFET is described in U.S. Pat. No. 4,811,075 issued to Klas H. Eklund for *High Voltage MOS Transistors*.

In another proposed device in the prior art, a thin layer lateral D-MOS transistor is in series with a single-sided JFET and with a parallel arrangement of a single-sided JFET and a double-sided JFET. This device utilizes three epitaxial layer to improve the device as a source follower. See U.S. Pat. No. 4,626,879 issued to Sel Colak for *Lateral Double-Diffused MOS Transistor Devices Suitable for Source-Follower Applications*.

For these and similar devices, it is very often necessary to provide some shielding in order to allow operation in high voltage applications.

SUMMARY OF THE INVENTION

In accordance with the preferred embodiment of the present invention, an insulated gate field effect transistor with an extended drain region is presented. The extended drain region includes a single-sided JFET and a double-sided JFET connected in parallel.

The insulated gate field effect transistor is built on a substrate of first conductivity type. A pocket (also called a well) of semiconductor material or second conductivity type is within the substrate adjoining a surface of the substrate. A body region of semiconductor material of the first conductivity type is within the pocket adjoining the surface of the substrate. Also, a source region of semiconductor material of the second conductivity type is within the body region adjoining the surface of the substrate. A drain contact region of semiconductor material of the second conductivity type is also within the pocket of semiconductor material adjoining the surface of the substrate.

A first intermediate region of semiconductor material of the first conductivity type is within the pocket of semiconductor material between the body region and the drain contact region. The first intermediate region adjoins the surface of the substrate. Also, a second intermediate region of semiconductor material of second conductivity type is within the pocket of semiconductor material between the body region and the drain contact region. The second intermediate region also adjoins the surface of the substrate. A portion of the second intermediate region extends between the first intermediate region and the surface of the substrate.

Alternately, the transistor may be regarded as a bipolar transistor with an extended collector region. The source region functions as an emitter, and the body region functions as a base.

In an alternate embodiment for high voltage devices, the pocket of semiconductor material of the second conductivity type is replaced by an epitaxial layer of the second conductivity type. Various isolation regions of the first conductivity type within the epitaxial layer are used as shielding to isolate each transistor pair from other devices on an integrated circuit.

For example, in a preferred embodiment, the shielding includes an isolation region of the first conductivity type diffused into the epitaxial layer. Surrounding the transistor pair is a first isolation region which extends from the surface of the epitaxial layer to the isolation layer. The first isolation region is of the first conductivity type. A buried layer of the second conductivity layer is placed below the first isolation layer. A second isolation regions surrounds the first isolation region. The second isolation region extends from the surface of the epitaxial layer to the buried layer. The second isolation region is of the second conductivity type. An epitaxial region surrounds the second isolation region. The epitaxial region extends from the surface of the epitaxial layer to a depth below the second isolation region. A third isolation region surrounds the epitaxial region. The third isolation region is of the first conductivity type and extends from the surface of the epitaxial layer to the substrate.

The present invention allows for significant reduction of "on" resistance while simplifying the manufacturing process over prior art circuits. For example, at low voltages (e.g., less than 100 volts), the present invention allows for "on" resistance which is reduced two to three times over the device disclosed by Colak. The additional shielding described in the preferred embodiments facilitates use of the present invention in high voltage applications.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a diagrammatic view of a lateral D-MOS/-bipolar transistor in accordance with the preferred embodiment of the present invention.

FIG. 2 is a schematic of the lateral D-MOS/bipolar transistor shown in FIG. 1 in accordance with the preferred embodiment of the present invention.

FIG. 3 is a diagrammatic view of a lateral D-MOS/-bipolar transistor in accordance with an alternate preferred embodiment of the present invention for high voltage devices.

FIG. 4 is a diagrammatic view of a lateral D-MOS/-bipolar transistor in accordance with another alternate preferred embodiment of the present invention for high voltage devices.

FIG. 5 shows an alternate shielding embodiment for the lateral D-MOS/bipolar transistors shown in FIGS. 1 through 4 in accordance with a preferred embodiment of the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

FIG. 1 shows a cross-sectional view of a lateral double-diffused insulated gate field effect transistor with an extended drain region which is a parallel combination of a single-sided JFET and a double-sided JFET formed on a semiconductor die 8.

A substrate 10 of first conductivity type is, for example, made of p⁻-type material doped with 5×10^{14} atoms per cubic centimeter. A typical depth of substrate 10 is 500 microns. A pocket 11 of material of second conductivity type is, for example, n-type material doped at 3×10^{12} atoms per square centimeter. Pocket 11 extends a depth of, for example, 5 microns below a surface 9 of die 8. The doping levels and dimensions given here and below are for a device with a breakdown voltage of approximately 300 volts.

Within pocket 11 a body region 12 of first conductivity type is, for example, p-type material doped at between 10^{17} and 10^{20} atoms per cubic centimeter. Body region 12 typically extends a depth of 1 micron below surface 9 of die 8. Within body region 12, a source region 13 of second conductivity type is, for example, n+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Source region 13, for example, extends 0.4 microns below surface 9 of die 8. Body region 12 may be electrically connected directly to substrate 10 by extending body region 12 outside pocket region 11.

A drain contact region 16 of second conductivity type is, for example, n+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Drain contact region 16, for example, extends 0.4 microns below surface 9 of die 8. A source contact 17 is placed on surface 9 in electrical contact with body region 12 and a source contact region portion of source region 13. A drain contact 19 is placed on surface 9 in electrical contact with drain contact region 16. An insulating layer 7 is placed on surface 9 of die 8. A gate contact 18 is placed on insulating layer 7 over a channel region portion of body region 12, as shown.

Between body region 12 and region 16 is a region 14 of second conductivity type. Region 14 is, for example n-type material doped at 2×10^{12} atoms per square centimeter. Region 14 extends downward from surface 9 to a depth of, for example 0.4 microns. Located below region 14 is a region 15 of first conductivity type. Region 15 is, for example, p-type material doped at 4×10^{12} atoms per square centimeter. Region 15 extends from surface 9 downward a depth of, for example 1 micron. Region 15 is connected to ground at surface 9 in a plane not shown in FIG. 1. A distance 6 between and edge of body region 12 and an edge of drain contact 16 is, for example 12 microns. A symmetry line 20 is used for placing a second half of the transistor in a mirror image to the first half shown in FIG. 1.

The circuit shown in FIG. 1, may also function as a bipolar transistor with region 13 functioning as an emitter, region 12 functioning as a base, and pocket 11, region 14 and region 16 functioning as an extended collector.

FIG. 2 shows a circuit diagram for the lateral double-diffused insulated gate field effect transistor with an extended drain region which is a parallel combination of a single-sided JFET and a double-sided JFET shown in FIG. 1. A transistor 22 is controlled by gate contact 18. Current through transistor 22 travels from source contact 17 through region 13 through body region 12 to region 11, shown in FIG. 1.

The extends drain region of transistor 22 includes a single-sided JFET 24 and a double-sided JFET 21 connected in parallel as shows. Current through single-sided JFET 24 passes through region 14 and through region 16 to drain contact 19. Region 15 serves as the single side of single-sided JFET 24. Current through double-sided JFET 21 passes through region 11 and through region 16 to drain contact 19. Region 15 and substrate 10 serve as the two sides of double-sided JFET 21.

The above-discussed design allows for significant reduction of resistance from source contact 17 to drain contact 19 when transistor 22 is "on", over circuits in the prior art. The present invention is also simpler to manufacture than related prior art devices.

FIG. 3 shows a cross-sectional view of a lateral double-diffused insulated gate field effect transistor with extended drain region in accordance with an alternate preferred embodiment of the present invention. The transistor shown in FIG. 3 is surrounded by isolation diffusion which is necessary in order to isolate the transistor from other devices on an integrated circuit.

A substrate 110 of first conductivity type is, for example, made of p⁻-type material doped with 5×10^{14} atoms per cubic centimeter. A typical depth of substrate 110 is 500 microns. A layer 111 of material of second conductivity type is, for example, n-type epitaxial material doped at 10^{15} atoms per cubic centimeter. Layer 111 extends a depth of, for example, 10 to 25 microns below a surface 109.

For a first half of the transistor, a body region 112 of first conductivity type is, for example, p-type material doped at between 10^{17} and 10^{20} atoms per cubic centimeter. Body region 112 typically extends a depth of 1 micron below surface 109. Within body region 112, a source region 113 of second conductivity type is, for example, n+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Source region 113, for example, extends 0.4 microns below surface 109.

A drain contact region 116 of second conductivity type is, for example, n+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Drain contact region 116, for example, extends 0.4 microns below surface 109.

A source contact 117 is placed on surface 109 in electrical contact with body region 112 and a source contact region portion of source region 113. A drain contact 119 is placed on surface 109 in electrical contact with drain contact region 116. An insulating layer 107 is placed on surface 109. A gate contact 118 is placed on insulating layer 107 over a channel region portion of body region 112, as shown.

Between body region 112 and region 116 is a region 114 of second conductivity type. Region 114 is, for example, n-type material doped at 2×10^{12} atoms per square centimeter. Region 114 extends downward from surface 109 to a depth of, for example 0.4 microns. Located below region 114 is a region 115 of first conductivity type. Region 115 is, for example, p-type material doped at 4×10^{12} atoms per square centimeter. Region 115 extends from surface 109 downward a depth of, for example 1 micron. Region 115 is connected to ground at surface 109 in a plane not shown in FIG. 1.

A second half of the transistor is a mirror image of the first half of the transistor with symmetry around drain contact region 116. For the second half of the transistor, a body region 132 of first conductivity type is, for example, p-type material. Within body region 132, a source region 133 of second conductivity type is, for example, n^+-type material.

A source contact 137 is placed on surface 109 adjacent to body region 132 and in electrical contact with source region 133. A gate contact 138 is placed on insulating layer 107 over a channel region portion of body region 132, as shown.

Between a body region 132 and region 116 is a region 134 of second conductivity type. Region 134 is, for example, n-type material. Located below region 134 is a region 135 of first conductivity type. Region 135 is connected to ground at surface 109 in a plane not shown in FIG. 3.

The transistor shown in FIG. 3, may also function as a bipolar transistor with region 113 and region 133 functioning as an emitter, region 112 and region 132 functioning as a base, and layer 111, region 114, region 134 and region 116 functioning as an extended collector.

An isolation region 141, an isolation region 142, an isolation region 143 and an isolation region 144, each of first conductivity type, provide isolation for the transistor from other devices. Isolation regions 141 through are, for example, of p-type material doped at between 10^{16} and 10^{19} atoms per cubic centimeter. Isolation region 141 and isolation region 143 are diffused down while isolation region 142 and isolation region 144 are diffused up.

When a device is either embedded in a well or an epitaxial layer, a severe problem can arise when the diode formed by the body region and the well (or epitaxial layer) is forward biased and the diode formed by the well region and the substrate is backed biased at a high negative voltage (e.g., less than −50 volts). Specifically, this can trigger a parasitic bipolar transistor where the body region will act as an emitter, the well (or epitaxial layer) will act as base and the substrate will act as a collector. The gain of such a parasitic bipolar transistor is typically more than 100; therefore, practically all the current will flow to the substrate creating a parasitic power dissipation through the substrate. To solve this issue, a layer of semiconductor material of opposite conductivity type from the conductivity type of the substrate may be buried under the well (or epitaxial layer) to drastically reduce the gain of the parasitic bipolar transistor. In many cases even this scheme does not result in sufficient isolation for optimal performance. In such cases, the isolation scheme shown in FIG. 4 may be utilized.

FIG. 4 shows a cross-sectional view of two lateral double-diffused insulated gate field effect transistors with extended drain regions where the transistors are additionally shielded from the substrate and other devices.

A substrate 210 of first conductivity type is, for example, made of p^--type material doped with 5×10^{14} atoms per cubic centimeter. A typical depth of substrate 210 is 500 microns. A layer 21 of material of second conductivity type is, for example, n-type epitaxial material doped at 10^{15} atoms per cubic centimeter. Layer 211 extends a depth of, for example, 12 to 17 microns below a surface 209.

For a first half of the transistor, a body region 212 of first conductivity type is, for example, p-type material doped at between 10^{17} and 10^{20} atoms per square centimeter. Body region 212 typically extends a depth of 1 micron below surface 209. Within body region 212, a source region 213 of second conductivity type is, for example, n^+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Source region 213, for example, extends 0.4 microns below surface 209.

A drain contact region 216 of second conductivity type is, for example, n^+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Drain contact region 216, for example, extends 0.4 microns below surface 209.

A source contact 217 is placed on surface 209 in electrical contact with body region 212 and a source contact region portion portion of source region 213. A drain contact 219 is placed on surface 209 in electrical contact with drain contact region 216. An insulating layer 207 is placed on surface 209. A gate contact 218 is placed on insulating layer 207 over a channel region portion of body region 212, as shown.

Between body region 212 and region 216 is a region 214 of second conductivity type. Region 214 is, for example, n-type material doped at 2×10^{12} atoms per square centimeter. Region 214 extends downward from surface 209 to a depth of, for example 0.4 microns. Located below region 214 is a region 215 of first conductivity type. Region 215 is, for example, p-type material doped at 4×10^{12} atoms per square centimeter. Region 215 extends from surface 209 downward a depth of, for example 1 micron. Region 215 is connected to ground at surface 209 in a plane not shown in FIG. 1.

A second half of the transistor is a mirror image of the first half of the transistor with symmetry around drain contact region 216. For the second half of the transistor, a body region 232 of first conductivity type is, for example, p-type material. Within body region 232, a source region 232, a source region 233 of second conductivity type is, for example, n^+-type material.

A source contact 237 is placed on surface 209 adjacent to body region 232 and in electrical contact with source region 233. A gate contact 238 is placed on insulating layer 207 over a channel region portion of body region 232, as shown.

Between body region 232 and region 216 is a region 234 of second conductivity type. Region 234 is, for example, n-type material. Located below region 234 is a region 235 of first conductivity type. Region 235 is connected to ground at surface 209 in a plane not shown in FIG. 4.

The transistor shown in FIG. 4, may also function as a bipolar transistor with region 213 and region 233 functioning as an emitter, region 212 and region 232 functioning as a base, and layer 211, region 214, region 234 and region 216 functioning as an extended collector.

Isolation layers and isolation regions isolate the transistor from the substrate and from other devices. Sur-

rounding the transistor shown in FIG. 4 is an isolation region 241, an isolation region 243 and an isolation region 290. Additionally, an isolation region 266 and an isolation region 267 are adjacent to a region 254 of epitaxial material of the second conductivity type. An isolation region 268 and an isolation region 269 are adjacent to a region 255 of epitaxial material of the second conductivity type. Additionally a sinker region 251 and a sinker region 253 are located as shown.

Isolation region 241, isolation region 243, isolation region 250, isolation region 266, isolation region 267, isolation region 268 and isolation region 269 are each of first conductivity type, for example, p-type material doped at between 10^{16} and 10^{20} atoms per cubic centimeter. Sinker region 251 and sinker region 253 are, for example of n^+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Region 254 and region 255 are, for example, of n-type epitaxial material doped at 10^{15} atoms per cubic centimeter.

In addition to Isolation region 250, a buried layer 249 of second conductivity type is placed to provide further isolation of the transistor from substrate 210. Buried layer 249 consists of, for example, n^+-type semiconductor material doped at between 10^{17} and 10^{19} atoms per cubic centimeter. Region 250 has a depth 261 of, for example, three microns. Buried layer 249 has a depth 262 of, for example, ten microns. Region 250 and buried layer 249 combine to effectively isolate substrate 210 from the transistor device even at high voltages.

FIG. 5 shows another shielding arrangement which isolates devices used in high voltage applications. A substrate 310 of first conductivity type is, for example, made of p^--type material doped with 5×10^{14} atoms per cubic centimeter. A typical depth of substrate 210 is 500 microns. A layer 350 of material of first conductivity type is, for example, p-type epitaxial material doped at between 5×10^{15} and 5×10^{16} atoms per cubic centimeter. Layer 350 extends a depth of, for example, 10 to 25 microns below a surface 309.

Active devices are placed within a well 311 of second conductivity type. Well 311 is, for example, n-type material doped at 5×10^{15} and 5×10^{16} atoms per cubic centimeter. Well 311 extends a depth of, for example, 5 microns below a surface 309.

Isolation layers and isolation regions isolate a device within well 311 from substrate 310 and from other devices. Immediately below well 311 is a region 351 which is in part of layer 350. Surrounding well 311 and region 351 is an isolation region 341, and an isolation region 342. Surrounding isolation region 341 and isolation region 342 are a sinker region 331 and a sinker region 332.

Isolation region 341 and isolation region 342 are each of first conductivity type, for example, p^+-type material doped at between 10^{17} and 10^{19} atoms per cubic centimeter. Sinker region 331 and sinker region 332 are, for example of n^+-type material doped at between 10^{17} and 10^{19} atoms per cubic centimeter.

A buried layer 349 of second conductivity type is placed to provide isolation of the device in well 311 from substrate 310. Buried layer 349 consists of, for example, n^+-type semiconductor material doped at between 10^{17} and 10^{19} atoms per cubic centimeter. Buried layer 349 has a depth of, for example, ten microns. Region 351 and buried layer 349 combine to effectively isolate substrate 310 from the device in well 311 even at high voltages greater than 50 volts.

The foregoing discussion discloses and describes merely exemplary methods and embodiments of the present invention. For example, in the above discussion the first conductivity type is n-type material and the second conductivity type is p-type material. Alternately, the first conductivity type could be p-type material and the second conductivity type could be n-type material. As will be understood by those familiar with the art, the invention may be embodied in other specific forms without departing from the spirit or essential characteristics thereof. Accordingly, the disclosure of the present invention is intended to be illustrative, but not limiting, of the scope of the invention, which is set forth in the following claims.

I claim:

1. A semiconductor device comprising:
a substrate of first conductivity type;
a pocket of semiconductor material of second conductivity type which adjoins a surface of the substrate;
a body region of semiconductor material of the first conductivity type which is within the pocket of semiconductor material and which adjoins the surface of the substrate;
a source region of semiconductor material of the second conductivity type, the source region being within the body region and adjoining the surface of the substrate;
a drain contact region of semiconductor material of the second conductivity type within the pocket of semiconductor material which adjoins the surface of the substrate;
a first intermediate region of semiconductor material of the first conductivity type which adjoins the surface of the substrate and which is located within the pocket of semiconductor material between the body region and the drain contact region; and,
a second intermediate region of semiconductor material of the second conductivity type which adjoins the surface of the substrate and which is located within the pocket of semiconductor material between the body region and the drain contact region, wherein a portion of the second intermediate region extends between the first intermediate region and the surface of the substrate.

2. A semiconductor device as in claim 1 wherein the substrate is electrically coupled to the body region by extending a portion of the body region out of the pocket of semiconductor material.

3. A semiconductor device as in claim 1 wherein the semiconductor device is a lateral double-diffused insulated gate field effect transistor with an extended drain region.

4. A semiconductor device as in claim 1 wherein the semiconductor device is a bipolar transistor, the source region functioning as an emitter, and the body region functioning as a base.

5. A semiconductor device comprising:
a drain contact;
a single-sided JFET having a first end electrically coupled to the drain contact and having a second end;
a double-sided JFET having a first end electrically coupled to the first end of the single-sided JFET and having a second end electrically coupled to the second end of the single-sided JFET;
a source contact;
a gate contact;

an insulated field effect transistor having a gate region coupled to the gate contact, having a source region electrically coupled to the source contact, and having a drain region electrically coupled to the second end of the single-sided JFET and to the second end of the double-sided JFET.

6. A semiconductor device as in claim 5 wherein the double-sided JFET comprises:

a first semiconductive path within a pocket of semiconductor material of second conductivity type, the pocket of semiconductor material being within a substrate of first conductivity type, wherein a first region of semiconductor material of first conductivity type is placed between the first semiconductive path and a surface of the substrate.

7. A semiconductor device as in claim 6 wherein the single-sided JFET comprises:

a second semiconductive path composed of a semiconductor material of second conductivity type; the second semiconductive path residing between the first region of semiconductor material and the surface of the substrate.

8. A semiconductor device as in claim 7 wherein the insulated gate field effect transistor comprises:

a body region of semiconductor material of the first conductivity type, the body region being within the pocket of semiconductor material wherein the body region adjoins the surface of the substrate and is separated from the gate contact by a layer of insulator placed on the surface of the substrate; and,

a source region of semiconductor material of the second conductivity type, the source region being within the body region and the source region being electrically coupled to the source contact.

9. A semiconductor device as in claim 5 wherein the double-sided JFET comprises:

a first semiconductive path within a layer of epitaxial material of second conductivity type, the layer of epitaxial material being deposited on a substrate of first conductivity type, wherein a first region of semiconductor material of first conductivity type is placed between the first semiconductive path and a surface of the layer of epitaxial material.

10. A semiconductor device as in claim 9 wherein the single-sided JFET comprises:

a second semiconductive path composed of semiconductor material of second conductivity type; the second semiconductive path residing between the first region of semiconductor material and the surface of the layer of epitaxial material.

11. A semiconductor device as in claim 10 wherein the insulated gate field effect transistor comprises:

a body region of semiconductor material of the first conductivity type, the body region being within the layer of epitaxial material wherein the body region adjoins the surface of the layer of epitaxial material and is separated from the gate contact by a layer of insulator placed on the surface of the layer of epitaxial material; and,

a source region of semiconductor material of the second conductivity type, the source region being within the body region and the source region being electrically coupled to the source contact.

12. A semiconductor device comprising:

a substrate of first conductivity type;

a layer of epitaxial material of second conductivity type deposited on a surface of the substrate;

a body region of semiconductor material of the first conductivity type which is within the layer of epitaxial material and which adjoins the surface of the layer of epitaxial material;

a source region of semiconductor material of the second conductivity type, the source region being within the body region and adjoining the surface of the layer of epitaxial material;

a drain contact region of semiconductor material of the second conductivity type within the layer of epitaxial material which adjoins the surface of the layer of epitaxial material;

a first intermediate region of semiconductor material of the first conductivity type which adjoins the surface of the layer of epitaxial material and which is located within the layer of epitaxial material between the body region and the drain contact region; and,

a second intermediate region of semiconductor material of the second conductivity type which adjoins the surface of the layer of epitaxial material and which is located within the layer of epitaxial material between the body region and the drain contact region, wherein a portion of the second intermediate region extends between the first intermediate region and the surface of the layer of epitaxial material.

13. A semiconductor device as in claim 12 wherein the semiconductor device is isolated from other semiconductor devices within the substrate by isolation layers of the first conductivity type within the layer of epitaxial material.

14. A semiconductor device as in claim 13 wherein the semiconductor device is isolated from the substrate by a first isolation layer of the first conductivity type diffused within the layer of epitaxial material and by a buried layer of the second conductivity type diffused within the layer of epitaxial material and below the first isolation layer.

15. A semiconductor device as in claim 12 wherein the semiconductor device is a lateral double-diffused insulated gate field effect transistor with an extended drain region.

16. A semiconductor device as in claim 12 wherein the semiconductor device is a bipolar transistor, the source region functioning as an emitter, and the body region functioning as a base.

17. A semiconductor device comprising:

a substrate of first conductivity type;

a layer of epitaxial material of second conductivity type deposited on a surface of the substrate;

a body region of semiconductor material of the first conductivity type which is within the layer of epitaxial material and which adjoins the surface of the layer of epitaxial material;

a source region of semiconductor material of the second conductivity type, the source region being within the body region and adjoining the surface of the layer of epitaxial material;

a drain contact region of semiconductor material of the second conductivity type within the layer of epitaxial material which adjoins the surface of the layer of epitaxial material;

a first isolation layer of the first conductivity type diffused in the layer of epitaxial material; and,

a buried layer of the second conductivity type diffused in the layer of epitaxial material and below the first isolation layer.

18. A semiconductor device as in claim 17 additionally comprising:

a first intermediate region of semiconductor material of the first conductivity type which adjoins the surface of the layer of epitaxial material and which is located within the layer of epitaxial material between the body region and the drain contact region; and,

a second intermediate region of semiconductor material of the second conductivity type which adjoins the surface of the layer of epitaxial material and which is located within the layer of epitaxial material between the body region and the drain contact region, wherein a portion of the second intermediate region extends between the first intermediate region and the surface of the layer of epitaxial material.

19. Shielding for a high power semiconductor device, the high power semiconductor device being placed in a layer of epitaxial material of second conductivity type deposited on a surface of a substrate of first conductivity type, the shielding comprising:

an isolation layer of the first conductivity type diffused in the layer of epitaxial material;

a first isolation region within the layer of epitaxial material and surrounding the high power semiconductor device, the first isolation region extending from the surface of the layer of epitaxial material to the isolation layer and the first isolation region being of the first conductivity type;

a buried layer of the second conductivity type diffused into the layer of epitaxial material and below the isolation layer;

a second isolation region surrounding the first isolation region, the second isolation region extending from the surface of the layer of epitaxial material to the buried layer and the second isolation region being of the second conductivity type;

an epitaxial region surrounding the second isolation region, the epitaxial region extending from the surface of the layer of epitaxial material to a depth below the second isolation region; and,

a third isolation region surrounding the epitaxial region, the third isolation region extending from the surface of the layer of epitaxial material and the third isolation region being of the first conductivity type.

20. A semiconductor device as in claim 17 wherein the semiconductor device is a lateral double-diffused insulated gate field effect transistor with an extended drain region.

21. A semiconductor device as in claim 17 wherein the semiconductor device is a bipolar transistor, the source region functioning as an emitter, and the body region functioning as a base.

22. A shielding for a high power semiconductor device within a layer of epitaxial material of first conductivity type deposited on a substrate of the first conductivity type, the shielding comprising:

a well of second conductivity type which adjoins a surface of the layer of epitaxial material, the high power semiconductor device being placed in the well;

a buried layer of the second conductivity type diffused into the layer of epitaxial material;

an isolation region of first conductivity type, within the layer of epitaxial material located above the buried layer and surrounding the well; and,

a sinker region of second conductivity type, placed above the buried layer and surrounding the isolation type.

* * * * *

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TITLE

DEVICE WHICH FUNCTIONS AS A LATERAL DOUBLE-DIFFUSED INSULATED GATE FIELD EFFECT TRANSISTOR OR AS A BIPOLAR TRANSISTOR

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PATENT

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Patent Application Transmittal Letter

ATTORNEY DOCKET NUMBER: 1003

INVENTOR(S): Klas H. Eklund

TITLE: DEVICE WHICH FUNCTIONS AS A LATERAL DOUBLE-DIFFUSED INSULATED GATE FIELD EFFECT TRANSISTOR OR AS A BIPOLAR TRANSISTOR

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[X] A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27

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[ ] FIRST PRESENTATION OF A MULTIPLE DEPENDENT CLAIM					$100	$ 0
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DEVICE WHICH FUNCTIONS AS A LATERAL DOUBLE-DIFFUSED INSULATED GATE FIELD EFFECT TRANSISTOR OR AS A BIPOLAR TRANSISTOR

Background

The present invention concerns a lateral double-diffused insulated gate field effect transistor where the extended drain region is a parallel combination of a single-sided junction field effect transistor (JFET) and a double-sided JFET. The present invention also relates to the construction of a bipolar transistor with an extended collector region. The present invention additionally relates generally to how metal-oxide-silicon (MOS) and/or a bipolar transistors can be effectively shielded from a substrate in a classic junction isolated technology.

Thin layer (resurfed) lateral double diffused metal oxide silicon (D-MOS) transistors have been shown to be an efficient means to integrate high voltage devices in the same die as low voltage control functions. See, for example, Sel Colak Effects of Drift Region Parameters on the Static Properties of Power LDMOS, IEEE Transactions on Electron Devices, VOL. ED-28, No. 12, pp. 1455-1466 (December 1981). This reference describes a device which can be considered a series combination of a D-MOS transistor and a single-sided JFET. The single-sided JFET functions as a pinch resistor. The JFET is commonly a thin n-type epitaxial layer deposited on top of a p-type substrate.

In order to improve thin layer lateral D-MOS transistors as a source follower and further reduce resistance when the device is "on", a surface layer of p-type doping has been added. The modified device can be considered a D-MOS

transistor in series with a double-sided JFET. See for example, A.W. Ludikhuize, High-Voltage DMOS and PMOS in Analog IC's, IEDM, pp. 81-84 (1982).

An efficient and simplistic way to incorporate a thin layer lateral high voltage MOS transistor which constitutes a series combination of a normal MOS transistor (not D-MOS) and a double-sided JFET is described in U.S. Patent Number 4,811,075 issued to Klas H. Eklund for High Voltage MOS Transistors.

In another proposed device in the prior art, a thin layer lateral D-MOS transistor is in series with a single-sided JFET and with a parallel arrangement of a single-sided JFET and a double-sided JFET. This device utilizes three epitaxial layers to improve the device as a source follower. See U.S. Patent Number 4,626,879 issued to Sel Colak for Lateral Double-Diffused MOS Transistor Devices Suitable for Source-Follower Applications.

For these and similar devices, it is very often necessary to provide some shielding in order to allow operation in high voltage applications.

Summary of the Invention

In accordance with the preferred embodiment of the present invention, an insulated gate field effect transistor with an extended drain region is presented. The extended drain region includes a single-sided JFET and a double-sided JFET connected in parallel.

The insulated gate field effect transistor is built on a substrate of first conductivity type. A pocket (also called a well) of semiconductor material of second conductivity type is within the substrate adjoining a surface of the substrate. A body region of semiconductor material of the first conductivity type is within the pocket adjoining the surface of the substrate. Also, a source region of semiconductor material of the second conductivity type is within the body region adjoining the surface of the substrate. A drain contact region of semiconductor material of the second conductivity type is also within the pocket of semiconductor material adjoining the surface of the substrate.

A first intermediate region of semiconductor material of the first conductivity type is within the pocket of semiconductor material between the body region and the drain contact region. The first intermediate region adjoins the surface of the substrate. Also, a second intermediate region of semiconductor material of second conductivity type is within the pocket of semiconductor material between the body region and the drain contact region. The second intermediate region also adjoins the surface of the substrate. A portion of the second intermediate region extends between the first intermediate region and the surface of the substrate.

Alternately, the transistor may be regarded as a bipolar transistor with an extended collector region. The source region functions as an emitter, and the body region functions as a base.

In an alternate embodiment for high voltage devices, the pocket of semiconductor material of the second conductivity type is replaced by an epitaxial layer of the second conductivity type. Various isolation regions of the first conductivity type within the epitaxial layer are used as shielding to isolate each transistor pair from other devices on an integrated circuit.

For example, in a preferred embodiment, the shielding includes an isolation region of the first conductivity type diffused into the epitaxial layer. Surrounding the transistor pair is a first isolation region which extends from the surface of the epitaxial layer to the isolation layer. The first isolation region is of the first conductivity type. A buried layer of the second conductivity layer is placed below the first isolation layer. A second isolation regions surrounds the first isolation region. The second isolation region extends from the surface of the epitaxial layer to the buried layer. The second isolation region is of the second conductivity type. An epitaxial region surrounds the second isolation region. the epitaxial region extends from the surface of the epitaxial layer to a depth below the second isolation region. A third isolation region surrounds the epitaxial region. The third isolation region is of the first conductivity type and extends from the surface of the epitaxial layer to the substrate.

The present invention allows for significant reduction of "on" resistance while simplifying the manufacturing process over prior art circuits. For example, at low voltages (e.g.,

less than 100 volts), the present invention allows for "on" resistance which is reduced two to three times over the device disclosed by Colak. The additional shielding described in the preferred embodiments facilitates use of the present invention in high voltage applications.

Brief Description of the Drawings

Figure 1 is a diagrammatic view of a lateral D-MOS/bipolar transistor in accordance with the preferred embodiment of the present invention.

Figure 2 is a schematic of the lateral D-MOS/bipolar transistor shown in Figure 1 in accordance with the preferred embodiment of the present invention.

Figure 3 is a diagrammatic view of a lateral D-MOS/bipolar transistor in accordance with an alternate preferred embodiment of the present invention for high voltage devices.

Figure 4 is a diagrammatic view of a lateral D-MOS/bipolar transistor in accordance with another alternate preferred embodiment of the present invention for high voltage devices.

Figure 5 shows an alternate shielding embodiment for the lateral D-MOS/bipolar transistors shown in Figures 1 through 4 in accordance with a preferred embodiment of the present invention.

Description of the Preferred Embodiment

Figure 1 shows a cross-sectional view of a lateral double-diffused insulated gate field effect transistor with an extended drain region which is a parallel combination of a single-sided JFET and a double-sided JFET formed on a semiconductor die 8.

A substrate 10 of first conductivity type is, for example, made of p^--type material doped with 5×10^{14} atoms per cubic centimeter. A typical depth of substrate 10 is 500 microns. A pocket 11 of material of second conductivity type is, for example, n-type material doped at 3×10^{12} atoms per square centimeter. Pocket 11 extends a depth of, for example, 5 microns below a surface 9 of die 8. The doping levels and dimensions given here and below are for a device with a breakdown voltage of approximately 300 volts.

Within pocket 11 a body region 12 of first conductivity type is, for example, p-type material doped at between 10^{17} and 10^{20} atoms per cubic centimeter. Body region 12 typically extends a depth of 1 micron below surface 9 of die 8. Within body region 12, a source region 13 of second conductivity type is, for example, n^+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Source region 13, for example, extends 0.4 microns below surface 9 of die 8. Body region 12 may be electrically connected directly to substrate 10 by extending body region 12 outside pocket region 11.

A drain contact region 16 of second conductivity type is, for example, n^+-type material doped at between 10^{18} and 10^{20} atoms per cubic centimeter. Drain contact region 16, for